LOT NUMBER	CONDES/TASK
MR030929	324-3230 03
PART NUMBER	REV.
WJ-9525-1	
DESCRIPTION	UM
MANUAL FOR WJ-9525-1	EA

INSTRUCTION MANUAL

FOR

WJ-9525-1 FDM DEMODULAT

MP MASTER

MA31062

WATKINS-JOHNSON

INSTRUCTION MANUAL

FOR

WJ-9525-1 FDM DEMODULATOR

WATKINS—JOHNSON COMPANY
700 Quince Orchard Road
Gaithersburg, Maryland 20878

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06399

ADDENDA

WJ-9525 and WJ-9525-1 FDM DEMODULATORS

The following changes should be incorporated into the WJ-9525 FDM Demodulator Instruction Manual.

1. Throughout the manual, reference to the WJ-9525 unit is to be understood as applying to the WJ-9525-1 in all aspects except tuning range, unless otherwise noted.

2. Section I - General Description
   a. Paragraph 1.1, General; Page 1-1
      1) Change paragraph to read:
      "This section contains a general description of the Watkins-Johnson 9525 and 9525-1 Frequency Division Multiplexing Demodulators, hereafter referred to as the WJ-9525(9525-1) FDM Demodulator or, the Demodulator..."

   b. Paragraph 1.2, General Description; Page 1-1
      1) Change last sentence to read:
      "The WJ-9525 Demodulator is capable of processing signals in the frequency band from 0 to 308 kHz. The WJ-9525-1 Demodulator is an essentially identical unit configured for a tuning range of 0 to 552 kHz.

   c. Table 1-1, Electrical Characteristics; Page 1-7
      1) Change the second item, Input Frequency Range, to read:
      "Input Frequency Range:
      WJ-9525 . . . . . 0 - 308 kHz
      WJ-9525-1 . . . . . 0 - 552 kHz"

      2) Change the sixth item, Mode, to read:
      "Mode . . . . . SSB Erect or Inverted"

3. Section IV - Theory of Operation
   a. Paragraph 4.2, Overall Functional Description; Page 4-1
      1) Change the first sentence to read:
      "Baseband input signals, from 200 Hz to 308 kHz (552 kHz for WJ-9525-1), are input..."

      2) Sixth paragraph, first sentence, change to read:
      "Baseband input signals, from 200 Hz to 308 kHz (552 kHz for WJ-9525-1), from the baseband..."

b. Paragraph 4.4, Control Unit (A2); Page 4-8
   1) Change Listing to read:
   "Type 796061 Motherboard (A2A1)
   Type 796045 CPU Processor and Memory Bus Expansion Logic (A2A1A1) - WJ-9525
   Type 796045-2 CPU Processor and Memory Bus Expansion Logic (A2A1A1) - WJ-9525-1
   Type 796046 Panel Interface..."

c. Paragraph 4.5.2.7.4, Voltage-Controlled Oscillator Q1; Page 4 -38
   1) Change paragraph to read:
   "...(Table 4-1) down to 19.10 MHz (16.60 MHz for WJ-9525-1) for a demodulator frequency of 308.00 kHz (552.00 kHz for WJ-9525-1). In the Invert Mode, VCO Q1 tunes from 18.16 MHz for a demodulator frequency of 000.000 kHz (Table 4-2) to 20.64 MHz (22.56 MHz for WJ-9525-1) for a demodulator frequency of 308.00 kHz (552.00 kHz for WJ-9525-1). The output..."

d. Table 4-1, Coarse Loop Assembly - Synthesizer Data (Erect Mode); Page 4-38
   1) Sixteenth line, Demodulator Frequency of 249.99, change column "U7" figures from 0100 to read:
   "0110"

   2) Add the following to the bottom of the table:

"*399.99	10	0000	0001	182	0 1	18.20	1.60001
*400.00	01	1111	1010	181	0 0	18.10	1.60000
*552.00	01	1110	0101	166	0 0	16.60	1.44800

*These figures apply to the WJ-9525-1 only."

e. Table 4-2, Coarse Loop Assembly - Synthesizer Data (Invert Mode); Page 4-39
   1) Add the following to the bottom of the Table:

"*363.50	10	1000	0010	263	1 0	21.04	2.36750
*353.51	10	1000	0011	264	1 1	21.12	2.36751
*552.00	10	1010	0001	282	1 1	22.56	2.55600

*These figures apply to the WJ-9525-1 only."

f. Table 4-3, VCO-Bandswitch Frequency Data; Page 4-39
   1) First line, Invert Mode, change to read:
   "21.12 - 22.56"

2) Third line, Erect Mode, change to read:
"18.20 - 19.60"

3) Fourth line, Erect Mode, change to read:
"16.60 - 18.10"

g. Paragraph 4.5.2.7.5, Bandswitch Switches Q2 and Q3; Page 4-39
1) Change last sentence of paragraph to read:
"The 18.16 MHz (16.60 MHz for WJ-9525-1) to 22.10 MHz (22.56 MHz for WJ-9525-1) output from Q4..."

h. Paragraph 4.5.2.7.6, Two-Modulus Prescaler U10; Page 4-39
1) Change first sentence to read:
"The 16.70 MHz (16.60 MHz for WJ-9525-1) to 22.10 MHz (22.56 MHz for WJ-9525-1) output from buffer..."

i. Paragraph 4.5.2.8.3, Voltage-Controlled Oscillator Q1; Page 4-42
1) Change paragraph to read:
"In the Erect Mode, the voltage-controlled oscillator Q1 tunes through various frequencies between 210.000 and 219.990 MHz as the demodulator frequency changes. See Table 4-4 for specifics. In the Invert Mode, the oscillator frequency ranges between 210.000 and 217.992 MHz, see Table 4-5. The output from VCO Q1..."

j. Table 4-4, Fine Loop Assembly-Synthesizer Data (Invert Mode); Page 4-43
1) Add the following to the bottom of the table:

"*363.50	0100	011	0010	26250	210.000	2.36750
*363.51	1110	011	0001	27249	217.992	2.36751
*552.00	0110	000	0000	26400	211.200	2.55600

*These figures apply to the WJ-9525-1 only."

k. Table 4-5, Fine Loop Assembly - Synthesizer Data (Erect Mode); Page 4-43
1) Add the following to the bottom of the table:

"*399.99	1001	110	0011	21999	219.99	1.60001
*400.00	0000	000	0000	21000	210.00	1.60000
*552.00	0010	000	0000	21200	212.00	1.44800

*These figures apply to the WJ-9525-1 only."

l. Paragraph 4.5.2.9, Type 796062 Main Loop Assembly (A1A3); Page 4-45

1) Change second paragraph to read:
"In the Erect Mode, RF inputs from the coarse loop are from 22.10 MHz down to 19.18 MHz (16.60 MHz for WJ-9525-1) and from the fine loop are from 2.1000 MHz up to 2.1999 MHz. In the Invert Mode, RF inputs from the coarse loop are from 18.16 MHz up to 20.64 MHz (22.56 MHz for WJ-9525-1) and from the fine loop are from 2.17992 MHz down to 2.1000 MHz. The LO strobe..."

2) Third paragraph, third line, change to read:
"...based on the 16.70 MHz (16.60 MHz for WJ-9525-1) to 22.56 MHz input..."

m. Figure 4-24, Main Loop Assembly Simplified Block Diagram; Page 4-46

1) Change indicated Erect and Invert frequencies to read as follows:

"

WJ-9525 - ERECT (20.000 - 16.920 MHz), INVERT (16.032 - 18.496 MHz)
WJ-9525-1 - ERECT (20.000 - 14.480 MHz), INVERT (16.032 - 20.448 MHz)

"

n. Paragraph 4.5.2.9.1, Phase Detector U1; Page 4-46

1) Change first sentence to read:
"...(Erect Mode) or 2.17992 MHz to 2.1000 (Invert Mode)..."

o. Paragraph 4.5.3.9.3, Voltage-Controlled Oscillator Q3; Page 4-47

1) Change paragraph to read:
"...(Table 4-6) down to 16.9200 MHz (14.4800 MHz for WJ-9525-1) for a demodulator frequency of 308.00 kHz (552.00 kHz for WJ-9525-1). In the Invert Mode, VCO Q3 tunes from 16.032 MHz for a demodulator frequency of 000.00 kHz (Table 4-7) up to 18.496 MHz (20.448 MHz for WJ-9525-1) for a demodulator frequency of 308.00 kHz (552.00 kHz for WJ-9525-1). The output..."

p. Table 4-6, Main Loop Assembly - Synthesizer Data (Erect Mode); Page 4-47

1) Seventh Line, change to read:

"0 0 9.9 9 | 1 1 | 1 9.9 0 0 1 | 1.9 9 0 0 1"

2) Eighth line, change to read:

"010.00	1 1	19.9000	1.99000"

3) Add the following to the bottom of the table:

"*399.99	0 1	16.0001	1.60001
*400.00	0 0	16.0000	1.60000
*552.00	0 0	14.4800	1.44800

*These figures apply to the WJ-9525-1 only."

q. Paragraph 4.5.2.9.4, Bandswitch Switches Q4 an Q5; Page 4-47

1) Change the last sentence to read:
"The 16.032 MHz (14.480 MHz for WJ-9525-1) to 20.000 MHz (20.448 MHz for WJ-9525-1) output from Q6..."

r. Table 4-7, Main Loop Assembly - Svnthesizer Data (Invert Mode); Page 4-48

1) Next to last line, Bandswitch Bits column, change to read:
"1 0"

2) Add the following to the bottom of the table:

"*363.50	1 0	18.94000	2.36750
*363.51	1 1	18.94008	2.36751
*552.00	1 1	20.44800	2.55600

*These figures apply to the WJ-9525-1 only."

s. Paragraph 4.5.2.9.5, Mixer U6; Page 4-48

1) Change first sentence to read:
"The 22.10 MHz to 19.18 MHz (16.60 MHz for WJ-9525-1) Erect Mode or 18.16 MHz to 20.64 MHz (22.56 MHz for WJ-9525-1) Invert Mode output from pin 14..."

2) Change second sentence to read:
"...the attenuator pad, the 16.032 MHz (14.480 MHz for WJ-9525-1) to 20.000 MHz (20.448 MHz for WJ-9525-1) output from Q6..."

t. Figure 4-26, Input Converter Assembly Functional Block Diagram; Page 4-50

1) Upper left hand corner of figure, change to read:
"1.692 - 2.0 MHz
2.004 - 2.312 MHz } WJ-9525

1.448 - 2.0 MHz
2.004 - 2.556 MHz } WJ-9525-1
LO input (from Main Loop Assembly)"

u. Paragraph 4.5.2.10. Type 796071 Input Converter Assembly (A1A4); Page 4-50
1) Fourth paragraph, first sentence, change to read: "The 2.000 MHz to 1.692 MHz (1.448 MHz for WJ-9525-1) Erect Mode or 2.004 MHz to 2.312 MHz (2.556 MHz for WJ-9525-1) Invert Mode, after amplification..."

4. Section V - Maintenance

a. Table 5-2, Demodulator Performance Standard; Page 5-2
1) Parameter 2., Performance Standard, change to read:
"...to 308 kHz (WJ-9525) or, to 552 kHz (WJ-9525-1)"

2) Parameter 3., Performance Standard, change to read:
"...288.88, 308.00 kHz, and 552.00 kHz."

3) Parameter 5., Performance Standard, change to read:
"...222.22 kHz, 308.00 kHz, and 552.00 kHz."

b. Paragraph 5.2.3.4, Controls/Indicators Performance Tests; Page 5-4
1) Items 7, 8, 9, 10, and 11, change last sentence to read:
"...between 000.00 and 308.00 limits (WJ-9525) and between 000.00 and 552.00 limits (WJ-9525-1)."

c. Paragraph 5.2.3.5, Baseband Frequency Response Test; Page 5-6
1) Item 5, change to read:
"...increase signal synthesizer output frequency to 308 kHz (WJ-9525) or 552 kHz (WJ-9525-1). Variation is less than 0.5 dB."

d. Paragraph 5.2.3.6, Baseband - Video Frequency (VF) Conversion Test; Page 5-7
1) Item 7, add to the listing:

"k.	553.000 kHz	552.00 kHz ERECT
l.	553.000 kHz	552.00 kHz INVERT"

2) Item 9, change to read:
"...output frequency to 309.000 kHz (WJ-9525), or 553.00 kHz (WJ-9525-1), tune demodulator unit 1 to 308.00 kHz (WJ-9525) or 552.00 kHz (WJ-9525-1), connect measuring leads..."

e. Figure 5-5, Demodulator Troubleshooting Flowchart (5 of 7); Page 5-23
1) First line, second block from left, change to read:
"Is response at 154 kHz and 308 kHz (552 kHz for WJ-9525-1) OK?"

f. Table 5-6, Program Operation; Page 5-31
1) First item, change to read:
"Frequency Tuning, 0 to 308 kHz (WJ-9525) or 0 to 552 kHz (WJ-9525-1)"

g. Table 5-7, Frequency Tuning, Page 5-32
1) Change table title to read:
"Table 5-7, Frequency Tuning, 0 to 552 kHz"

h. Paragraph 5.3.4.7.2, Tuning Voltages, Resolution, Range, and Accuracy; Page 5-80
1) Item 15, change to read:
"...unit to 308.00 kHz (WJ-9525) or 552.00 kHz (WJ-9525-1)."

2) Item 16, change to read:
"...frequency to 309.00 kHz (WJ-9525) or 553.00 kHz (WJ-9525-1) and output level..."

5. Section VI - Replacement Parts List
a. Subsection 6.5.2.1.1, Type 796045 CPU Processor & Memory, Page 6-29
1) REF DESIG, U2, Manufacturer's Part No., change to read:
"841054 (WJ-9525)
841073 (WJ-9525-1)

INSTRUCTION MANUAL

FOR

WJ-9525 FDM DEMODULATOR

This document and subject matter disclosed herein are proprietary items to which Watkins-Johnson Company retains the exclusive right of dissemination, reproduction, manufacture and sale.

This document is provided to the individual or using oganization for their use alone in the direct support of the associated equipment unless permission for further disclosure is expressly granted in writing.

WATKINS-JOHNSON COMPANY

700 QUINCE ORCHARD ROAD

GAITHERSBURG, MARYLAND 20878

WARNING

This equipment employs voltages which are dangerous and may be fatal if contacted. Extreme caution should be exercised when working on this equipment with any protective covers removed.

WARNING

Recommended cleaning procedures in Section V of this document involve the use of 1, 1, 1-trichloroethane (methyl chloroform). Avoid breathing high concentrations of vapors and prolonged skin contact with this cleaning solvent. Overexposure may lead to a slight anesthetic feeling, possible irritation to eyes, nose, and throat. Continued exposure can result in headaches, fatigue, dizziness, nausea, and gradual suppression of consciousness.

EQUIPMENT AND PROCEDURAL SAFETY

Equipment and procedural safety practices are paramount to both the user and manufacturer of this equipment. As a result, the following general guidelines are presented as a reminder to prevent possible personnel injury and equipment damage.

1. Preventive and corrective maintenance on this equipment, with the protective covers removed and power applied, should be performed by skilled technicians familiar with this equipment.

2. With equipment power off and with the equipment power cord disconnected from a power source, there is a possibility that capacitors in the equipment may still be charged.

3. Replace defective equipment power fuses with fuses of the same size and type which are both specified on the equipment and in this publication.

The following list is provided to define the differences between the equipment name and model number as presented in this commercial manual and the equipment's tagged military nomenclature in accordance with JETDS.

	Equipment Name and Model Number	Military Nomenclature
1.	FDM Demodulator, WJ-9525	Demultiplexer, TD-1323(V)1/G
2.	Control Rack Frame, WJ-9525/CRF	Power Supply/Amplifier, PP-7639/G
3.	Control Unit, WJ-9525/CU	Control Unit, C-10827/G
4.	Demodulator Unit, WJ-9525/DU	Demultiplexer, TD-1324/G

TABLE OF CONTENTS

SECTION I

DESCRIPTION

Paragraph		Page
1.1	General	1-1
1.2	General Description	1-1
1.2.1	WJ-9525/CU Control Unit	1-1
1.2.2	WJ-9525/DU Demodulator Unit	1-1
1.2.3	WJ-9525/CRF Control Rack Frame	1-1
1.3	Mechanical Description	1-1
1.4	Demodulator Assemblies	1-2
1.4.1	Control Unit	1-2
1.4.2	Demodulator Unit	1-2
1.4.3	Control Rack Frame	1-2
1.5	Equipment Supplied	1-2
1.6	Equipment Required But Not Supplied	1-2
1.7	Equipment Specifications	1-7
1.8	Operating Temperature Range	1-7

SECTION II

INSTALLATION

2.1	General	2-1
2.2	Receipt Inspection	2-1
2.3	Unpacking, Inspection and Inventory	2-1
2.4	Pre-Installation Inspection	2-1
2.5	Installation Requirements	2-1
2.5.1	Equipment Location	2-1
2.5.2	Power Requirements	2-3
2.5.3	Ground Requirements	2-3
2.6	Installation	2-3
2.6.1	Rear Panel Connections	2-3
2.6.1.1	Control Rack Frame	2-3
2.7	Preparation for Use	2-5
2.7.1	Establish Demodulator Address	2-6
2.8	Preparation for Storage or Shipment	2-7
2.8.1	Environment	2-7
2.8.2	Packaging	2-7
2.8.2.1	Original Packaging	2-7
2.8.2.2	Other Packaging	2-8

TABLE OF CONTENTS (Cont'd)

SECTION III

OPERATION

Paragraph		Page
3.1	General	3-1
3.2	Controls and Indicators	3-1
3.2.1	Control Rack Frame	3-1
3.2.2	Control Unit	3-1
3.2.3	Demodulator Unit	3-1
3.3	Baseband Signal Distribution Amplifier Assembly A1A1	3-4
3.4	Initial Start-up and Operation	3-5
3.5	Start-up Operation	3-6
3.6	Local Selection of a Demodulator Unit	3-7
3.7	Remote Programming Information	3-7
3.7.1	Bi-directional bus	3-7
3.7.1.1	Data Lines	3-8
3.7.1.2	Transfer Lines	3-8
3.7.1.2.1	NRFD	3-8
3.7.1.2.2	NDAC	3-8
3.7.1.2.3	DAV	3-10
3.7.1.3	Control and Status Line	3-11
3.7.1.3.1	ATN	3-11
3.7.1.3.2	SRQ	3-11
3.7.2	Data Transfer	3-11
3.7.3	Programming Codes	3-12
3.7.4	Basic Control Functions from a 9825 Controller	3-13
3.7.5	Available Functions	3-14
3.7.6	Demodulator Select	3-14
3.7.7	Set Modes, ERE-INV, REM-LOC, AGC-MAN	3-14
3.7.8	Set Frequency	3-14
3.7.9	Read Demodulator Status	3-14
3.7.10	Read Bus Status (SERVICE REQUEST)	3-15
3.8	Shut Down and Interrupted Power	3-15

SECTION IV
THEORY OF OPERATION

Paragraph		Page
4.1	General	4-1
4.2	Overall Functional Description	4-1
4.3	Control Rack Frame (A1)	4-3
4.3.1	Functional Description	4-3
4.3.2	Type 796074 Baseband Signal Distribution Amplifier Assembly (A1A1)	4-3

TABLE OF CONTENTS (Cont'd)

SECTION IV

THEORY OF OPERATION (Cont'd)

Paragraph		Page
4.3.2.1	Type 796065 Baseband Signal Distribution Amplifier PC Assembly (A1A1A1 and A1A1A2)	4-3
4.3.3	Demodulator Power Supply	4-5
4.3.3.1	Power Input Circuitry	4-6
4.3.4	Type 766001 Power Supply Assembly (A1A2)	4-6
4.3.5	Power Regulation Circuitry	4-7
4.3.6	Type 76060 Reference Generator Assembly (A1A3)	4-7
4.3.6.1	Part 380084 Reference Generator PC Assemby (A1A3A1)	4-7
4.4	Control Unit (A2)	4-8
4.4.1	Functional Description	4-8
4.4.2	Type 796061 Motherboard Assembly (A2A1)	4-9
4.4.2.1	Type 796045 CPU Processor and Memory Assembly (A2A1A1)	4-9
4.4.2.1.1	Functional Description	4-9
4.4.2.1.2	Circuit Description.	4-15
4.4.2.2	Type 796046 Panel Interface and Demodulator Control Assembly (A2A1A2)	4-17
4.4.2.2.1	Functional Description	4-17
4.4.2.2.2	Circuit Description.	4-17
4.4.2.3	Type 796047-1 IEEE 488/RS-232 I/O Assembly (A2A1A3)	4-21
4.4.2.3.1	Functional Description	4-21
4.4.2.3.2	Circuit Description.	4-23
4.5	Demodulator Units (A3, A4, A5, A6)	4-24
4.5.1	Functional Description	4-24
4.5.2	Type 796070 Motherboard Assembly (A1)	4-26
4.5.2.1	4-Bit Latch U3	4-31
4.5.2.2	8-Bit Shift/Storage Registers U10, U11, U12, U8, and U6	4-31
4.5.2.3	Driver U7	4-32
4.5.2.4	Logic Gates U1 and U2	4-34
4.5.2.5	2 MHz Reference Buffer U4	4-34
4.5.2.6	Digital-To-Analog Converter U9, Amplifier U5.	4-35
4.5.2.7	Type 796064 Coarse Loop Assembly (A1A2)	4-35
4.5.2.7.1	Decoder Logic U2A, U2B, U2D and Divide-By-Counters U1, U4A	4-36
4.5.2.7.2	Phase Detector U5	4-37
4.5.2.7.3	Filter U6	4-38
4.5.2.7.4	Voltage-Controlled Oscillator Q1.	4-38
4.5.2.7.5	Bandswitch Switches Q2 and Q3	4-38
4.5.2.7.6	Two-Modulus Prescaler U10	4-39
4.5.2.7.7	Programmable Counters U7, U8, and U9.	4-40
4.5.2.8	Type 796063 Fine Loop Assembly (A1A1)	4-41
4.5.2.8.1	Phase Detector U1	4-42
4.5.2.8.2	Filter U2	4-42
4.5.2.8.3	Voltage-Controlled Oscillator Q1.	4-42

TABLE OF CONTENTS (Cont'd)

SECTION IV

THEORY OF OPERATION (Concluded)

Paragraph		Page
4.5.2.8.4	Divide-By-10 Counter U11	4-42
4.5.2.8.5	Divide-By-10 Counter U12	4-42
4.5.2.8.6	Divide-By-10/11 Counter U9	4-44
4.5.2.8.7	Divide-By-10 Counter U8	4-44
4.5.2.8.8	Programmable Counters U3 Through U7	4-44
4.5.2.9	Type 796062 Main Loop Assembly (A1A3)	4-45
4.5.2.9.1	Phase Detector U1	4-46
4.5.2.9.2	Filter U2	4-47
4.5.2.9.3	Voltage-Controlled Oscillator Q3	4-47
4.5.2.9.4	Bandswitch Switches Q4 and Q5	4-47
4.5.2.9.5	Mixer U6	4-48
4.5.2.9.6	Divide-By-Five/Four Counter U4	4-48
4.5.2.9.7	Divide-By-Two Counter U5A	4-48
4.5.2.10	Type 796071 Input Converter Assembly (A1A4)	4-49
4.5.2.10.1	LO Amplifier Q9	4-50
4.5.2.10.2	Double-Balanced Mixer U1	4-50
4.5.2.10.3	2 MHz IF Amplifier Q10	4-51
4.5.2.10.4	Low-Pass Filter (L1 Through L3, C1 and C2)	4-51
4.5.2.10.5	Attenuator Pads	4-51
4.5.2.10.6	Gain-Controlled Amplifier Q11	4-52
4.5.2.10.7	Baseband AGC Amplifier U2	4-52
4.5.2.11	Type 796066 Attenuator Control Assembly (A1A5)	4-52
4.5.2.11.1	Comparator U1	4-53
4.5.2.11.2	Quad 2-Line-to-1 Line Multiplexer (U3)	4-54
4.5.2.11.3	Switch Drivers U4A Through U4D, U5A and U5B	4-54
4.5.2.11.4	Audio Switch U7	4-54
4.5.2.11.5	AGC/MAN Switch U6	4-54
4.5.2.12	Type 796069 IF Demodulator Assembly (A1A6)	4-55
4.5.2.12.1	Gain-Controlled Amplifier Q1	4-55
4.5.2.12.2	Product Detector U1	4-56
4.5.2.12.3	Audio Amplifiers U2C and U2D	4-57
4.5.2.12.4	AGC IF Amplifier Q4	4-57
4.5.2.12.5	Average Detector CR2	4-57
4.5.2.12.6	Buffer U2A	4-57
4.5.2.12.7	AGC Integrator U2B	4-57
4.5.3	Type 796067 Display Board Assembly (A2) and Type 796068 Display Driver Assembly (A3)	4-57
4.5.3.1	8-Bit Shift/Storage Registers U1 and U2	4-58
4.5.3.2	Display Drivers U3 Through U7	4-59
4.5.3.3	Type 796067 Display Board Assembly (A2)	4-59
4.5.3.3.1	Displays DS1 through DS5	4-61
4.5.3.3.2	BCD-to-Decimal Decoder/Driver U1	4-61

TABLE OF CONTENTS (Cont'd)

SECTION V

MAINTENANCE

Paragraph		Page
5.1	General	5-1
5.2	Preventive Maintenance	5-1
5.2.1	Cleaning and Lubrication	5-1
5.2.1.1	Cleaning	5-1
5.2.1.2	Lubrication	5-2
5.2.2	Inspection	5-2
5.2.3	Performance Test Procedures	5-2
5.2.3.1	Introduction	5-2
5.2.3.2	Performance Standards	5-2
5.2.3.3	General Guidelines	5-3
5.2.3.4	Controls/Indicators Performance Tests	5-4
5.2.3.5	Baseband Frequency Response Test	5-5
5.2.3.6	Baseband - Video Frequency (VF) Conversion Test	5-6
5.2.3.7	Manual and AGC Control Range Test	5-8
5.2.3.8	Noise and Crosstalk Test	5-9
5.2.3.9	Remote Operational Checkout	5-10
5.3	Corrective Maintenance	5-13
5.3.1	Guidelines	5-13
5.3.2	Operator Maintenance Procedures	5-14
5.3.3	Troubleshooting/Fault Isolation Procedures	5-14
5.3.4	Subassembly Corrective Maintenance	5-29
5.3.4.1	General	5-29
5.3.4.2	Subassembly Fault Isolation Procedures	5-29
5.3.4.3	Digital Section Testing	5-29
5.3.4.4	Program Operation	5-31
5.3.4.5	Program Listing	5-49
5.3.4.6	Test Points and Variable Components	5-76
5.3.4.7	Adjustment/Alignment Procedures	5-77
5.3.4.7.1	Manual and Automatic Gain Levels and Control	5-77
5.3.4.7.2	Tuning Voltages, Resolution, Range and Accuracy	5-79
5.3.5	Repair Techniques	5-81
5.3.5.1	General	5-81
5.3.5.2	Printed Circuit Board and Assembly Removal, Installation	5-82
5.3.5.3	Component Removal	5-82
5.3.5.4	Component Installation	5-82
5.3.5.5	Printed Circuit Board Repair and Cleaning	5-82

TABLE OF CONTENTS (Cont'd)

SECTION VI

REPLACEMENT PARTS LIST

Paragraph		Page
6.1	Unit Numbering Method	6-1
6.2	Reference Designation Prefix	6-1
6.3	List of Manufacturers	6-1
6.4	Parts List	6-5
6.5	Type WJ-9525 Demodulator, Main Chassis	6-6
6.5.1	Type WJ-9525/CRF Control Rack Frame A1	6-7
6.5.1.1	Type 796074 Baseband Signal Distribution Amplifier A1A1	6-13
6.5.1.1.1	Part 796065 Baseband Distribution Amplifier A1A1A1, A1A1A2	6-15
6.5.1.2	Type 766001 Power Supply A1A2	6-19
6.5.1.3	Type 796060 Reference Generator Assembly A1A3	6-20
6.5.1.3.1	Part 380084 Reference Generator A1A3A1	6-21
6.5.2	Type WJ-9525/CU Control Unit A2	6-23
6.5.2.1	Type 796061 Motherboard, Control Unit, A2A1	6-27
6.5.2.1.1	Type 796045 CPU Processor and Memory A2A1A1	6-29
6.5.2.1.2	Type 796046 Panel Interface/Demodulator Control A2A1A2	6-31
6.5.2.1.3	Type 796047-1 IEEE 488/RS-232 I/O Module A2A1A3	6-35
6.5.3	Type WJ-9525/DU Demodulator Unit A3 through A6	6-37
6.5.3.1	Type 796070 Motherboard, Demodulator Unit, A3A1 through A6A1	6-39
6.5.3.1.1	Type 796063 Fine Loop A3A1A1 through A6A1A1	6-41
6.5.3.1.2	Type 796064 Coarse Loop A3A1A2 through A6A1A2	6-45
6.5.3.1.3	Type 796062 Main Loop A3A1A3 through A6A1A3	6-49
6.5.3.1.4	Type 796071 Input Converter/Attenuator A3A1A4 through A6A1A4	6-53
6.5.3.1.5	Type 796066 Attenuator Control A3A1A5 through A6A1A5	6-57
6.5.3.1.6	Type 796069 IF Demodulator A3A1A6 through A6A1A6	6-59
6.5.3.2	Type 796067 Display Board A3A2 through A6A2	6-63
6.5.3.2.1	Type 796068 Display Driver A3A3 through A6A3	6-65

SECTION VII

SCHEMATIC DIAGRAMS

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

Figure		Page
1-0	WJ-9525 FDM Demodulator	1-0
1-1	WJ-9525 FDM Demodulator Block Diagram	1-2
1-2	Demodulator Assemblies	1-3
1-3	Control Rack Frame Assemblies	1-4
1-4	Control Unit Assemblies	1-5
1-5	Typical Demodulator Unit Assemblies	1-6
2-1	WJ-9525 FDM Demodulator Critical Dimensions Drawing	2-2
2-2	Control Rack Frame, Rear Panel	2-3
3-1	Control Rack Frame Front Panel	3-1
3-2	Control Unit Front Panel	3-2
3-3	Demodulator Unit Front Panel	3-3
3-4	Transfer Lines Timing	3-9
4-1	Demodulator Functional Block Diagram	4-1
4-2	Baseband Signal Distribution Amplifier Block Diagram	4-4
4-3	Baseband Signal Distribution Amplifier PC Assembly Block Diagram	4-5
4-4	Demodulator Power Supply Block Diagram	4-6
4-5	Reference Generator PC Assembly Block Diagram	4-8
4-6	Control Unit Functional Block Diagram	4-9
4-7	Control Unit Digital Hardware Block Diagram	4-11
4-8	CPU Processor and Memory Functional Block Diagram	4-13
4-9	Microprocessor Pin Assignments	4-15
4-10	Processor Memory and I/O Maps	4-16
4-11	Panel Interface and Demodulator Control Functional Block Diagram	4-19
4-12	IEEE 488/RS-232 I/O Functional Block Diagram	4-22
4-13	Demodulator to IEEE 488 Bus Handshake Timing	4-23
4-14	Demodulator Unit Functional Block Diagram	4-25
4-15	LO Synthesizer Functional Block Diagram	4-27
4-16	Demodulator Unit Motherboard Assembly Block Diagram	4-29
4-17	Serial Data Format	4-32
4-18	Driver U7 Functional Diagram	4-33
4-19	Coarse Loop Assembly Simplified Block Diagram	4-35
4-20	Divide-By-Counters U1, U4A Timing	4-37
4-21	Divide-By-Counters U7, U8, U9, and U10, Typical ÷191	4-40
4-22	Fine Loop Assembly Simplified Block Diagram	4-41
4-23	Divide-By-Counters U3 Through U7, Typical ÷21800	4-45
4-24	Main Loop Assembly Simplified Block Diagram	4-46
4-25	Divide-By-Ten/Eight Counters U4 and U5A Timing Diagram	4-49
4-26	Input Converter Assembly Functional Block Diagram	4-50
4-27	6 dB Attenuator Pad A Circuit Diagram	4-51
4-28	Attenuator Control Assembly Functional Block Diagram	4-53
4-29	Audio Switch U7 Circuit Diagram	4-55
4-30	IF Demodulator Functional Block Diagram	4-56
4-31	Display Driver Functional Block Diagram	4-58
4-32	Display Board Functional Block Diagram	4-60

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

Figure		Page
5-1	Test Setup, Baseband Frequency Response and Output Level Test	5-5
5-2	Test Setup, Baseband - VF Conversion Test	5-6
5-3	Test Setup, Manual/AGC Control Range Test	5-8
5-4	Test Setup, Noise and Crosstalk Test	5-10
5-5	Demodulator Troubleshooting Flow Chart	5-15
5-6	Adjustment Setup, Manual and Automatic Gain Levels and Control	5-77
5-7	Adjustment Setup, Tuning Voltages, Resolution, Range and Accuracy	5-79
6-1	WJ-9525 Demodulator, Front View, Location of Components	6-6
6-2	WJ-9525/CRF Control Rack Frame (A1), Front View, Location of Components	6-8
6-3	WJ-9525/CRF Control Rack Frame (A1), Rear View, Location of Components	6-8
6-4	WJ-9525/CRF Control Rack Frame (A1), Top View, Location of Components	6-11
6-5	WJ-9525/CRF Control Rack Frame (A1), Bottom View, Location of Components	6-12
6-6	Type 796074 Baseband Signal Distrubtion Amplifier (A1A1), Front View, Location of Components	6-13
6-7	Type 796074 Baseband Signal Distribution Amplifier (A1A1), Rear View, Location of Components	6-14
6-8	Type 796065 Baseband Signal Distribution Amplifier (A1A1A1, A1A1A2), Location of Components	6-17
6-9	Type 766001 Power Supply (A1A2), Location of Components	6-18
6-10	Type 796060 Reference Generator Assembly (A1A3), Top View, Location of Components	6-20
6-11	Part 380084 Reference Generator Assembly (A1A3A1), Location of Components	6-22
6-12	WJ-9525/CU Control Unit (A2), Front View, Location of Components	6-24
6-13	WJ-9525/CU Control Unit (A2), Rear View, Location of Components	6-24
6-14	WJ-9525/CU Control Unit (A2), Top View, Location of Components	6-25
6-15	Type 796061 Motherboard, Control Unit, (A2A1), Location of Components	6-26
6-16	Type 796045 CPU Processor and Memory (A2A1A1), Location of Components	6-28
6-17	Type 796046 Panel Interface/Demodulator Control (A2A1A2), Location of Components	6-33
6-18	Type 796047-1 IEEE 488/RS-232 I/O Module (A2A1A3), Location of Components	6-34
6-19	WJ-9525/DU Demodulator Unit (A3 through A6), Front View, Location of Components	6-36
6-20	WJ-9525/DU Demodulator Unit (A3 through A6), Right Side View, Location of Components	6-37

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

Figure		Page
6-21	Type 796070 Motherboard, Demodulator Unit, (A3A1 through A6A1), Location of Components	6-38
6-22	Type 796063 Fine Loop (A3A1A1 through A6A1A1), Location of Components	6-43
6-23	Type 796064 Coarse Loop (A3A1A2 through A6A1A2), Location of Components	6-44
6-24	Type 796062 Main Loop (A3A1A3 through A6A1A3), Location of Components	6-48
6-25	Type 796071 Input Converter/Attenuator (A3A1A4 through A6A1A4), Location of Components	6-52
6-26	Type 796066 Attenuator Control (A3A1A5 through A6A1A5), Location of Components	6-56
6-27	Type 796069 IF Demodulator (A3A1A6 through A6A1A6), Location of Components	6-58
6-28	Type 796067 Display Board (A3A2 through A6A2), Location of Components	6-62
6-29	Type 796068 Display Driver (A3A3 through A6A3), Location of Components	6-64
7-1	WJ-9525/CRF Control Rack Frame (A1) Schematic Diagram	7-1
7-2	Type 796074 Baseband Signal Distribution Amplifier (A1A1) Schematic Diagram	7-7
7-3	Type 796065 Baseband Signal Distribution Amplifier PC Assembly (A1A1A1, A1A1A2) Schematic Diagram	7-9
7-4	Type 766001 Power Supply (A1A2) Schematic Diagram	7-13
7-5	Type 796060 Reference Generator (A1A3) Schematic Diagram	7-15
7-6	Part 380084 Reference Generator PC Assembly (A1A3A1) Schematic Diagram	7-17
7-7	WJ-9525/CU Control Unit (A2) Schematic Diagram	7-21
7-8	Type 796061 Motherboard (A2A1) Schematic Diagram	7-25
7-9	Type 796045 CPU Processor and Memory (A2A1A1) Schematic Diagram	7-31
7-10	Type 796046 Panel Interface and Demodulator Control (A2A1A2) Schematic Diagram	7-41
7-11	Type 796047-1 IEEE 488/RS-232 Input/Output (A2A1A3) Schematic Diagram	7-47
7-12	WJ-9525/DU Demodulator Unit (A3, A4, A5, A6) Schematic Diagram	7-53
7-13	Type 796070 Motherboard (A3A1) Schematic Diagram	7-55
7-14	Type 796063 Fine Loop (A3A1A1) Schematic Diagram	7-61
7-15	Type 796064 Coarse Loop (A3A1A2) Schematic Diagram	7-65
7-16	Type 796062 Main Loop (A3A1A3) Schematic Diagram	7-69
7-17	Type 796071 Input Converter (A3A1A4) Schematic Diagram	7-73
7-18	Type 796066 Attenuator Control (A3A1A5) Schematic Diagram	7-79
7-19	Type 796069 IF Demodulator (A3A1A6) Schematic Diagram	7-83
7-20	Type 796067 Display Board (A3A2) Schematic Diagram	7-87
7-21	Type 796068 Display Driver (A3A3) Schematic Diagram	7-89

TABLE OF CONTENTS (Cont'd)

LIST OF TABLES

Table		Page
1-1	Electrical Characteristics	1-7
2-1	Control Rack Frame Rear Panel Connections and Controls	2-3
2-2	Switch (A3S3) to Address Settings	2-6
3-1	Control Rack Frame Front Panel Controls and Indicators	3-2
3-2	Control Unit Front Panel Controls	3-2
3-3	Demodulator Unit Front Panel Controls and Indicators	3-4
3-4	Baseband Input Channel to Output Switching	3-5
3-5	Relationship of ATN Line and Transfer Lines	3-10
3-6	Programming Codes	3-12
3-7	Special Action Codes, Universal Commands	3-13
3-8	Programming Examples	3-13
4-1	Coarse Loop Assembly - Synthesizer Data (Erect Mode)	4-38
4-2	Coarse Loop Assembly - Synthesizer Data (Invert Mode)	4-39
4-3	VCO - Bandswitch Frequency Data	4-39
4-4	Fine Loop Assembly - Synthesizer Data (Invert Mode)	4-43
4-5	Fine Loop Assembly - Synthesizer Data (Erect Mode)	4-43
4-6	Main Loop Assembly - Synthesizer Data (Erect Mode)	4-47
4-7	Main Loop Assembly - Synthesizer Data (Invert Mode)	4-48
4-8	Input Level vs. Attenuator Pad State	4-52
4-9	U1A Through U1D State - Input Voltage	4-53
4-10	Multiplexer U3 Outputs - Attenuation Levels	4-54
4-11	Display Driver to Display Relationships	4-59
4-12	Decoder/Driver U1 Inputs/Outputs to DS11 Relationships	4-61
5-1	Preventive Maintenance Procedure and Adjust Schedules	5-1
5-2	Demodulator Peformance Standards	5-2
5-3	Operationally Identified Fault Symptoms	5-13
5-4	DU Select Voltages	5-15
5-5	Attenuator Control Voltages	5-25
5-6	Program Operation	5-31
5-7	Frequency Tuning, 0 to 308 kHz	5-32
5-8	Erect/Invert Selection	5-33
5-9	Manually Adjustable Gain/AGC Selection	5-34
5-10	Local/Remote Operator Request	5-35
5-11	Initialization and Power Up	5-36
5-12	Remote Talker and Listener	5-37
5-13	Jump Table	5-38
5-14	ASCII Status Conversion	5-39
5-15	Operational and Miscellaneous Routines	5-40
5-16	Index of Labels and RAM Locations	5-45
5-17	Description of Major Routines	5-47
5-18	Test Points and Variable Components	5-76

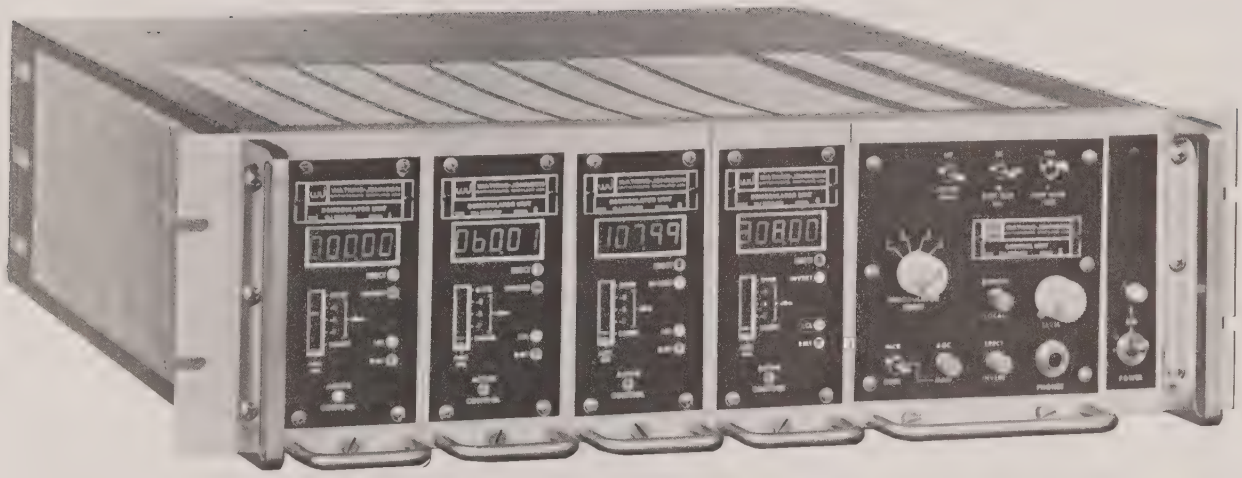


Figure 1-0. WJ-9525 FDM Demodulator

SECTION I
GENERAL DESCRIPTION

1.1 GENERAL

This section contains a general description of the Watkins-Johnson 9525 Frequency Division Multiplexing Demodulator, hereafter referred to as the WJ-9525 FDM Demodulator or, the Demodulator. Included in this section are tables of technical, environmental, and physical characteristics, equipment supplied, and equipment required, but not supplied information.

1.2 GENERAL DESCRIPTION

The WJ-9525 FDM Demodulator (Figure 1-0) consists of one WJ-9525/CU Control Unit and four WJ-9525/DU Demodulator Units all of which are plugged into and contained by a WJ-9525/CRF Control Rack Frame. The Demodulator is capable of processing signals in the frequency band from 0 to 308 kHz.

1.2.1 WJ-9525/CU CONTROL UNIT

The WJ-9525/CU Control Unit, hereafter referred to as the control unit, provides the means of selection, tuning and control of the four WJ-9525/DU Demodulator Units in either a local or remote mode of operation. The control unit (Figure 1-1), in the local mode, contains all of the operator related controls for the Demodulator. Operator changes to the control unit front panel controls result in the applicable changes to the selected demodulator unit. These changes are displayed on the selected demodulator unit's front panel indicators.

1.2.2 WJ-9525/DU DEMODULATOR UNIT

The WJ-9525/DU Demodulator Unit, hereafter referred to as the demodulator unit, is an independent Single Side Band (SSB) demodulator with high stability and tuning accuracy provided by frequency synthesizers. The demodulator unit indicators provide, in both local and remote modes, the selected frequency, control mode, sideband, and gain mode.

1.2.3 WJ-9525/CRF CONTROL RACK FRAME

The WJ-9525/CRF Control Rack Frame, hereafter referred to as the control rack frame, supports the control unit and demodulator units and provides the electrical interface between the control unit and demodulator units. It also contains the demodulator power supply, baseband distribution, and the IEEE standard 488 I/O port.

1.3 MECHANICAL DESCRIPTION

The Demodulator mounts in a standard 19-inch equipment rack, occupies 5.22 inches of vertical space, and extends approximately 20.0 inches into the rack (extension or overall depth of equipment measurement being made to faces of rear protective handles). The control unit and demodulator unit housings are constructed of aluminum with the overall weight of a complete Demodulator being approximately 50 pounds (22.73 Kg). All operating controls and indicators are on the front panels and all input and output cables are connected to associated connectors on the rear panel. The ac line fuses, line voltage selector switches, and bridge circuit switches are also on the rear panel.

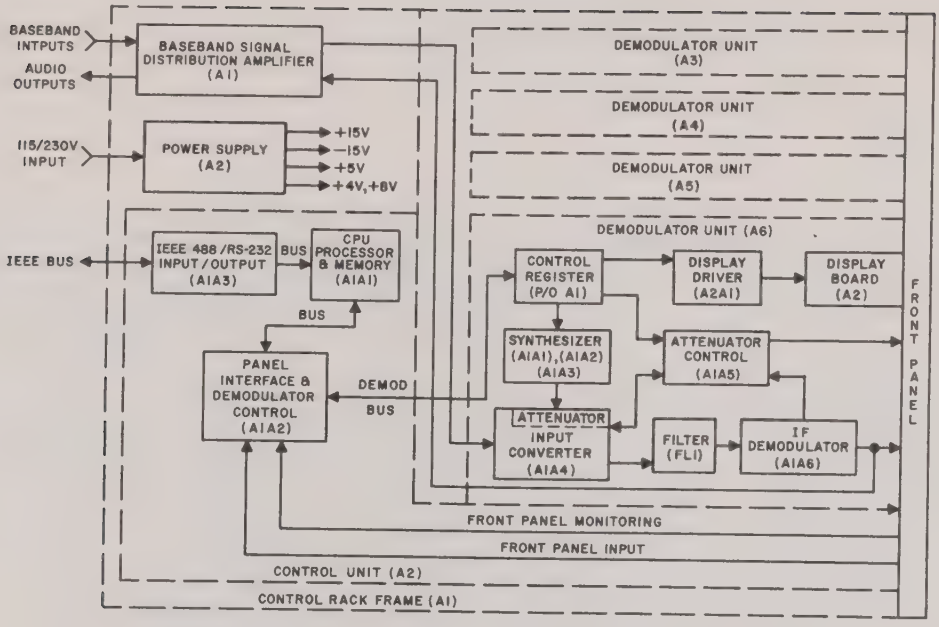


Figure 1-1. WJ-9525 FDM Demodulator Block Diagram

1.4 DEMODULATOR ASSEMBLIES

The Demodulator consists of a control unit, four demodulator units, and the control rack frame, which are illustrated and identified in Figure 1-2.

1.4.1 CONTROL UNIT

The control unit's major assemblies are illustrated and identified in Figure 1-4.

1.4.2 DEMODULATOR UNIT

A demodulator unit's major assemblies are illustrated and identified in Figure 1-5.

1.4.3 CONTROL RACK FRAME

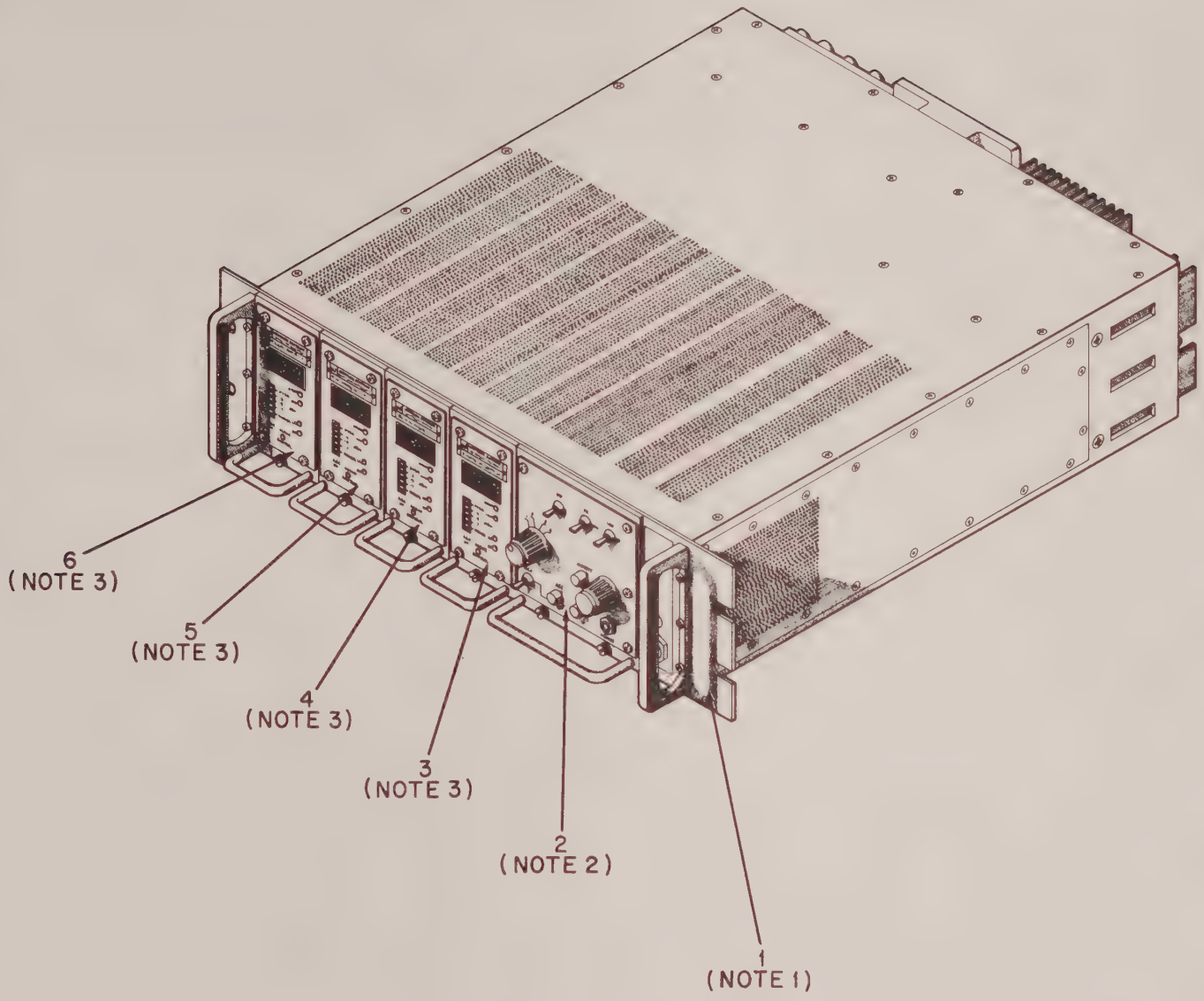
The control rack frame's major assemblies are illustrated and identified in Figure 1-3.

1.5 EQUIPMENT SUPPLIED

The equipment supplied consists of the WJ-9525 FDM Demodulator, its mating audio output connector, line cord, extender cables, and cards.

1.6 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The Demodulator requires a 93 Ω baseband input. Headphones (600 Ω or greater impedance) such as Telex Model HM-5 are required for use with the front panel audio output. A



LEGEND:

1. CONTROL RACK FRAME (A1)
2. CONTROL UNIT (A2)
3. DEMODULATOR UNIT 4 (A6)
4. DEMODULATOR UNIT 3 (A5)
5. DEMODULATOR UNIT 2 (A4)
6. DEMODULATOR UNIT 1 (A3)

NOTES:

1. SEE ALSO FIGURE 1-3.
2. SEE ALSO FIGURE 1-4.
3. SEE ALSO FIGURE 1-5.

Figure 1-2. Demodulator Assemblies

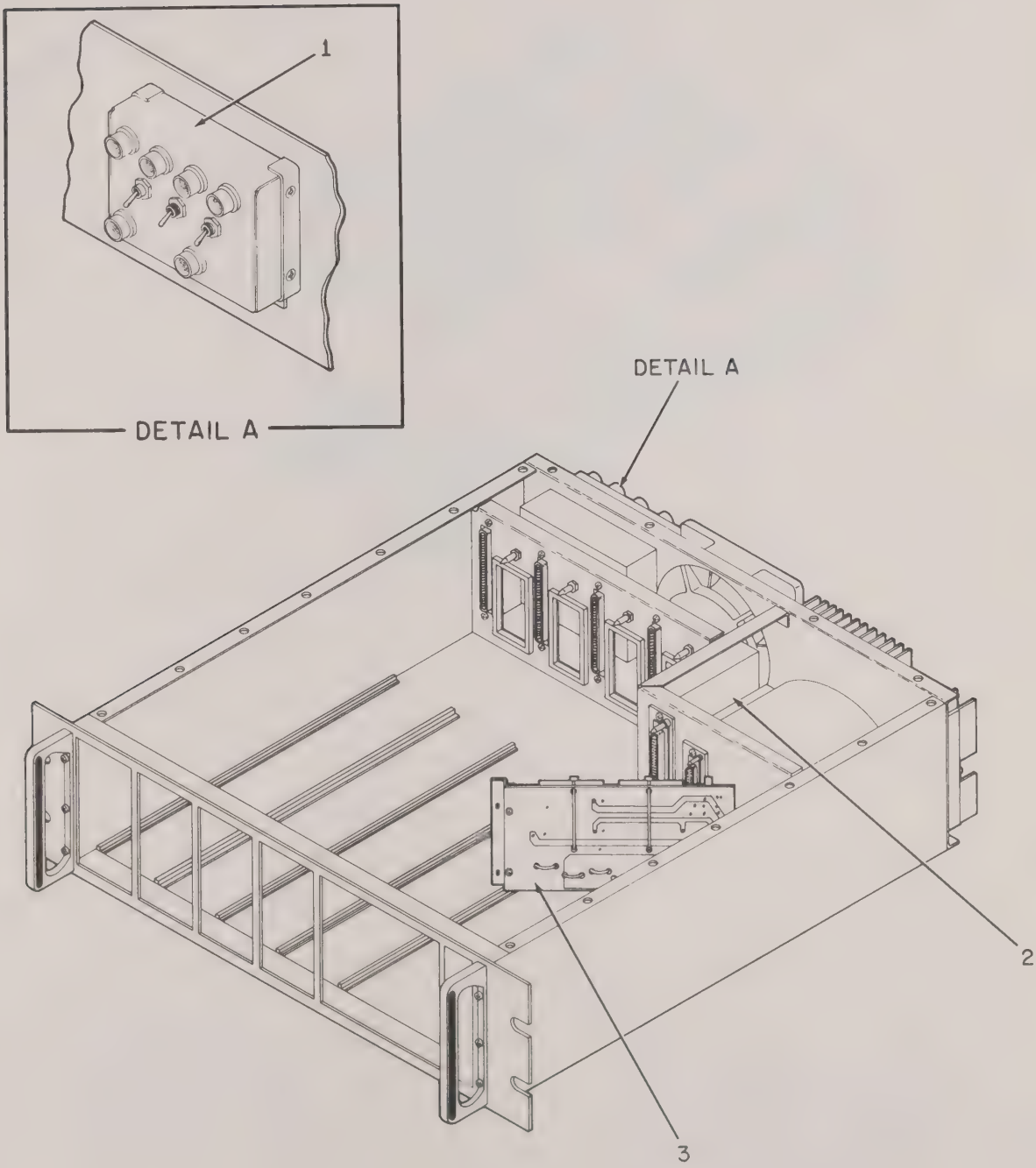


Figure 1-3. Control Rack Frame Assemblies

computer or other control device must be used for remote operation, and other rear panel input and output interfacing devices must be supplied by the user according to particular demodulator application. Refer to Section II of this manual for installation procedures.

1.7 EQUIPMENT SPECIFICATIONS

Table 1-1 lists the specifications and electrical characteristics of the Demodulator.

1.8 OPERATING TEMPERATURE RANGE

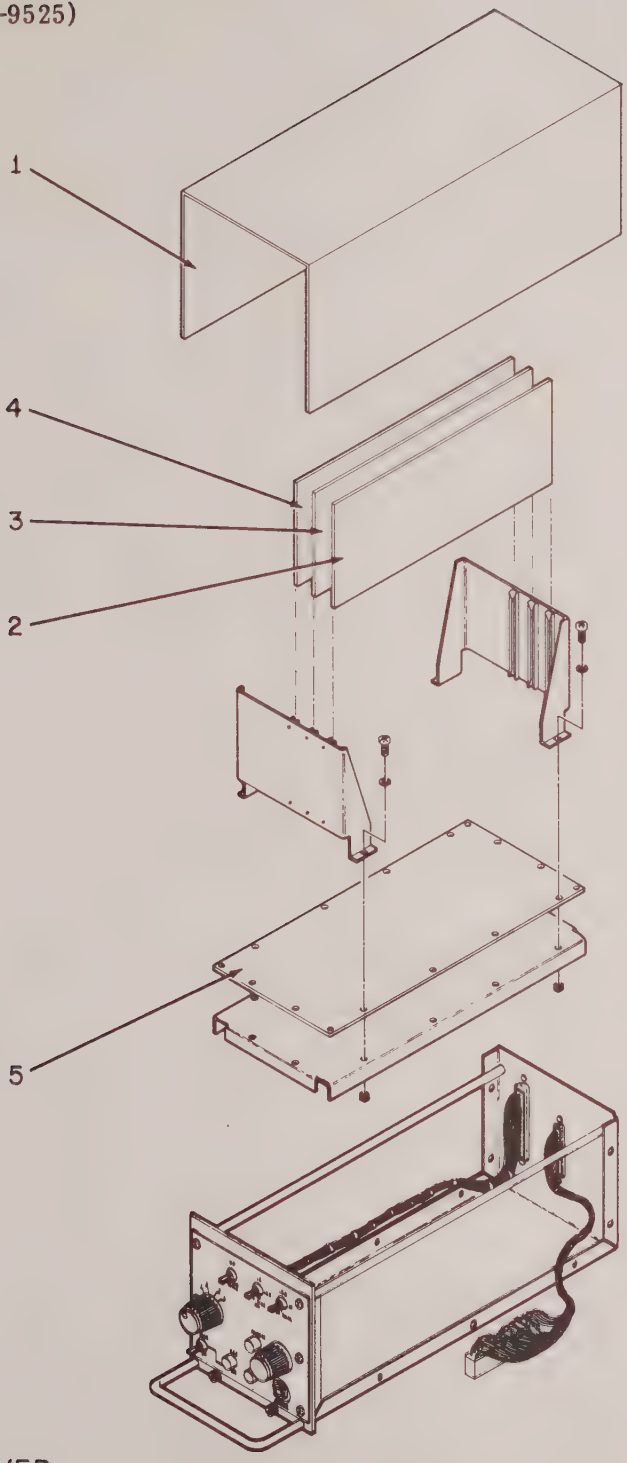
The operating temperature range of the Demodulator is from 0°C to 50°C (32.0°F to 122.0°F). The nominal operating temperature is 25°C ±10°C (77°F ±18°F).

Table 1-1. Electrical Characteristics

Number of Inputs:	
WJ-9525/CRF	Four: bridging via rear-panel switches
Input Frequency Range	0 to 308 kHz
Input Impedance	93 ohms unbalanced
Input Level	-25 dBm nominal, single tone
Input Level Range	-45 to -5 dBm, manual or AGC
Mode	FDM SSB upright or inverted
Output Frequency Response (±1 dB)	200 to 3400 Hz minimum
Group Delay Response	300 µs, maximum 200 to 3200 Hz
Tuning Step Resolution	10, 100, 1000 Hz (selectable)
Tuning Rate	1, 10, 100 Steps/Sec (selectable)
Tuning	10 Hz per least significant digit, synthesizer controlled
Frequency Readout	LED, 10 Hz resolution
Output Level	-5 dBm nominal, into 600 ohm
Output Impedance	600 ohms unbalanced
Headphone Output Level	10 mV, minimum, into 600 ohm load
Gain Control	Manual or Automatic (AGC) (selectable)
Gain Control Range	40 dB minimum
AGC Characteristics	Fast Attack, Slow Release, Audio output changes 3 dB maximum for specified input range
Adjacent Channel Rejection	45 dB, minimum @ 400 Hz from 200 and 3400 Hz output
Crosstalk Between Demodulators	Minimum of 60 dB
Residual Noise Above 4 kHz	60 dB, minimum below nominal output
Residual Noise, Zero Tuning	40 dB, minimum below nominal output
Noise Power Ratio	45 dB, minimum with input noise load of -38.5 to +1.5 dBm and noise bandwidth of 12 to 300 kHz
Incidental Frequency Modulation	2 Hz RMS maximum in a 4 kHz bandwidth
Harmonic Distortion of Output	50 dB, minimum below nominal output level

Table 1-1. Electrical Characteristics (continued)

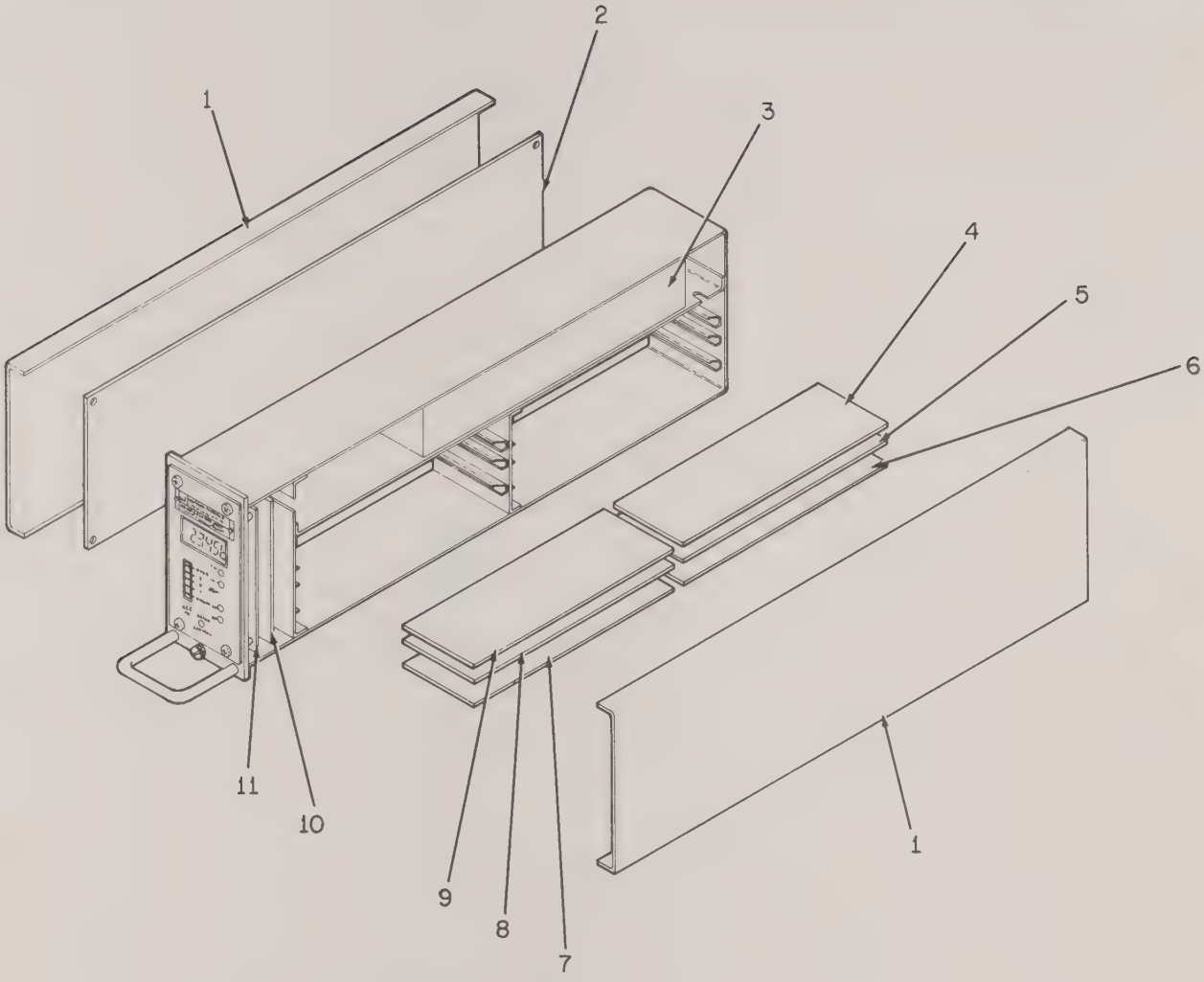
Reference Frequency Stability	1 PPM per day, after 30 minute warmup
Reference Frequency Accuracy	2 PPM per year, (reference-oscillator internally adjusted)
External Reference	When connected, requires 1 MHz, +10 to -5 dBm, 50 ohms
Input Power	115/230 Vac, ±10%, 50 to 400 Hz
Power Consumption	120 watts, approximately



LEGEND:

1 COVER
2. IEEE 488/RS 232 I/O ASSEMBLY (A1A3)
3. CPU PROCESSOR & MEMORY ASSEMBLY (A1A1)
4. PANEL INTERFACE & DEMODULATOR CONTROL ASSEMBLY (A1A2)
5. MOTHERBOARD ASSEMBLY (A1)

Figure 1-4. Control Unit Assemblies



LEGEND:

1. COVER
2. MOTHERBOARD ASSEMBLY (AXA1)
3. DELAYED EQUALIZED FILTER (AXFL1)
4. IF DEMODULATOR ASSEMBLY (AXA1A6)
5. ATTENUATOR CONTROL ASSEMBLY (AXA1A5)
6. INPUT CONVERTER ASSEMBLY (AXA1A4)
7. MAIN LOOP ASSEMBLY (AXA1A3)
8. COARSE LOOP ASSEMBLY (AXA1A2)
9. FINE LOOP ASSEMBLY (AXA1A1)
10. DISPLAY DRIVER ASSEMBLY (AXA3)
11. DISPLAY BOARD ASSEMBLY (AXA2)

Figure 1-5. Typical Demodulator Unit Assemblies

SECTION II

INSTALLATION

2.1 GENERAL

This section includes information on receipt inspection, unpacking, installation, and initial pre-operational adjustment. Also included are details of system ground requirements and preparation for storage or shipment.

2.2 RECEIPT INSPECTION

Inspect the shipping container for obvious damage. If the shipping container is damaged, attempt to have the carrier's agent present while the contents of the container are unpacked, checked for completeness, and the equipment inspected for mechanical damage. If it is not feasible to have the carrier's agent present, retain the damaged shipping container and equipment padding for the carrier's inspection.

2.3 UNPACKING, INSPECTION AND INVENTORY

The equipment was thoroughly inspected and adjusted for optimum performance prior to packing for shipment. It should be, therefore, ready for use upon receipt. After unpacking, inventory the equipment against the packing slip. Contact Watkins-Johnson Company, Gaithersburg, Maryland, or your Watkins-Johnson representative with details of any shortage.

After unpacking and taking inventory, visually inspect all exterior surfaces for dents, scratches, or any obvious signs of mechanical damage. If external damage is found, remove the protective covers and inspect internal components for signs of mechanical damage.

2.4 PRE-INSTALLATION INSPECTION

Prior to installation, remove the protective cover and inspect internal components. Check electrical connectors for possible loosened connections and check plug-in components, such as printed wiring boards, for proper installation in their receptacles.

2.5 INSTALLATION REQUIREMENTS

2.5.1 EQUIPMENT LOCATION

The Demodulator contained in its control rack frame, illustrated in Figure 2-1, is designed for mounting in a standard 19-inch equipment rack. The control rack frame occupies 5.22 inches of vertical rack space and extends approximately 20.0 inches into the rack (extension or depth of equipment measurement being made to faces of rear protective handles). When installed in a standard 19-inch equipment rack, the control rack frame should be installed in a location which allows a free flow of air through and around the rack-associated control unit and demodulator units. Also, the installation should allow access to the rear panel of the control rack frame for the purposes of making electrical/interface connections and ease of access to rear panel mounted switches and fuses.

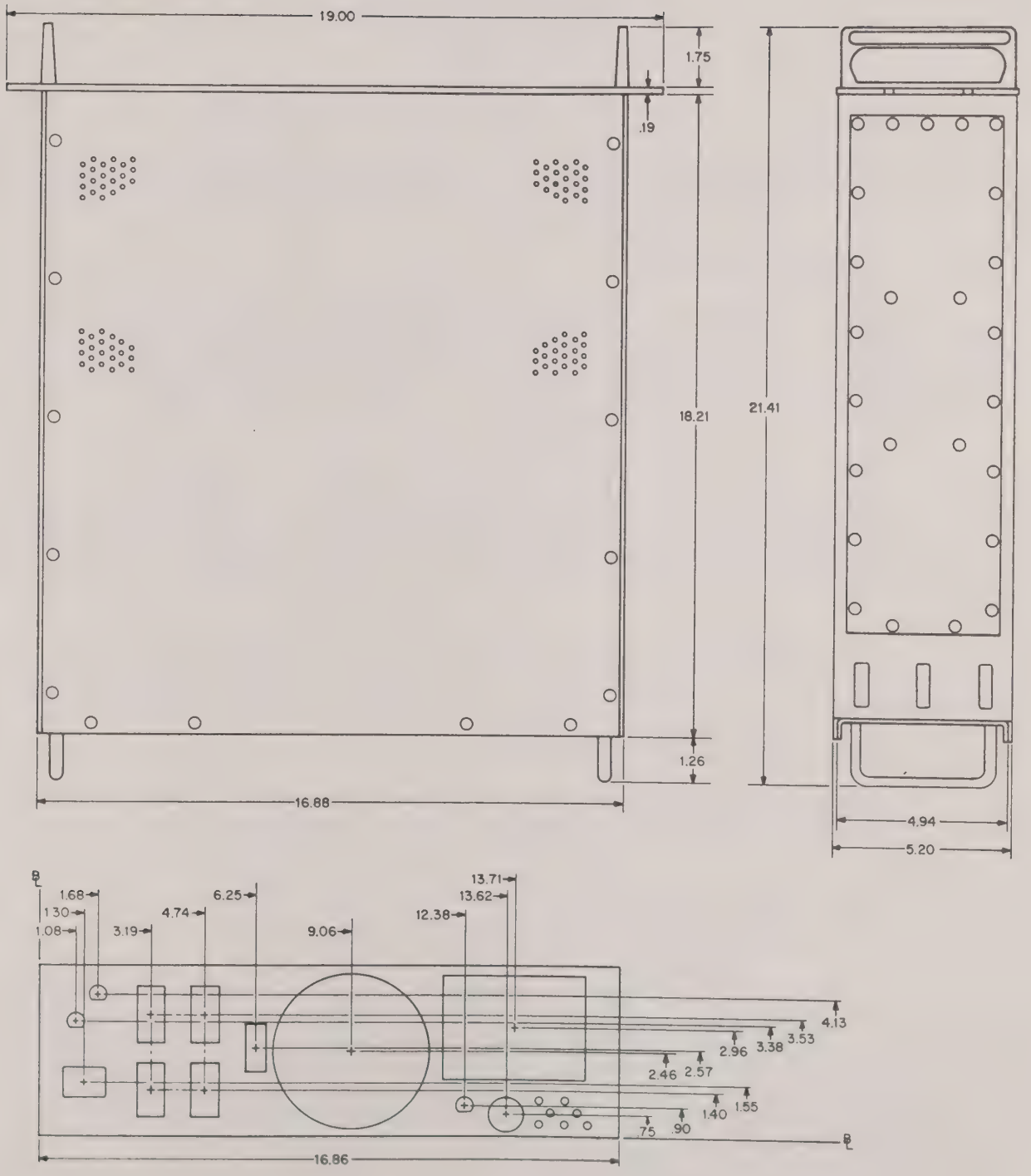


Figure 2-1. WJ-9525 FDM Demodulator Critical Dimensions Drawing

2.5.2 POWER REQUIREMENTS

The Demodulator requires a power source of 115 or 230 Vac ±10%, 50 to 400 Hz, single phase. Power consumption is approximately 120 watts.

2.5.3 GROUND REQUIREMENTS

In addition to the standard facility ground via the 115 or 230 Vac power connection, each control rack frame has a ground lug on its rear panel.

2.6 INSTALLATION

2.6.1 REAR PANEL CONNECTIONS

2.6.1.1 Control Rack Frame

The control rack frame rear panel connections and switches are illustrated in Figure 2-2 and described in Table 2-1.

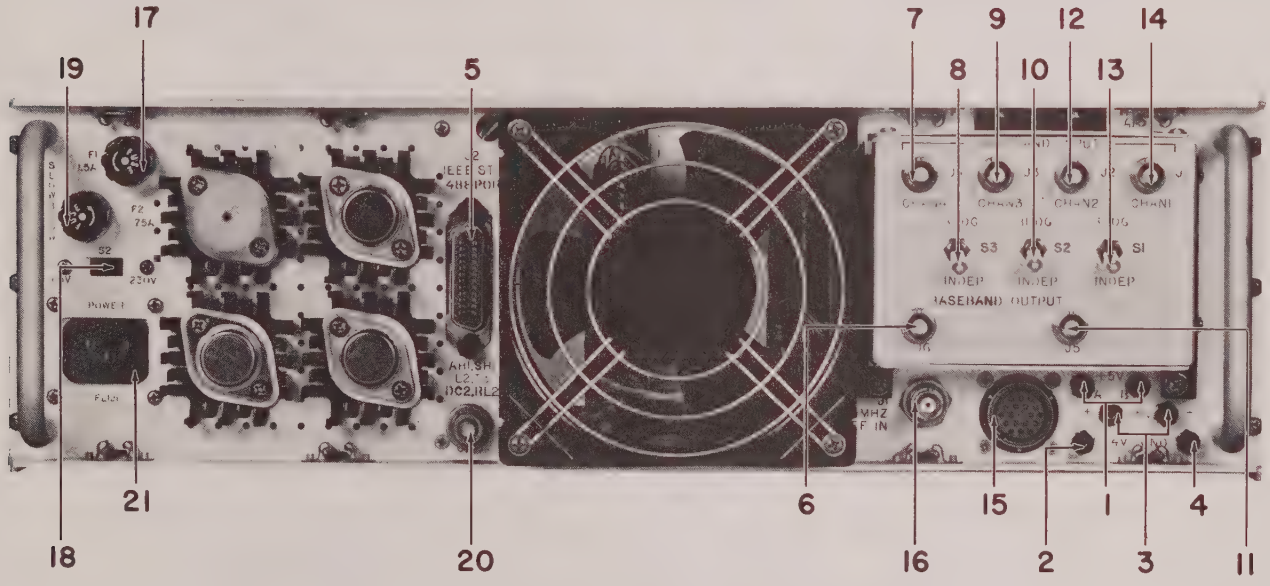


Figure 2-2. Control Rack Frame, Rear Panel

Table 2-1. Control Rack Frame Rear Panel Connections and Controls

Index No.	Panel Nomenclature	Function/Description
1	SUPPLIES, +5A, +5B	Test point, enables measurement of +5 Vdc.
2	SUPPLIES, +4	Test point, enables measurement of +4 Vdc.

Table 2-1. Control Rack Frame Rear Panel Connections and Controls (Cont'd)

Index No.	Panel Nomenclature	Function/Description
3	SUPPLIES, +15, -15	Test point, enables measurement of +15 and -15 Vdc.
4	SUPPLIES, COM	Test point, establishes ground potential.
5	IEEE STD 488 PORT	Remote control interface.
6	BASEBAND OUTPUT J6	Connector, enables additional demodulation of selected baseband.
7	BASEBAND INPUT CHAN 4 J4	Connector, enables baseband input for demodulator unit 4 and for BASEBAND output J6.
8	BRDG S3 BRDG/INDEP	Two position switch, used with switches S1 and S2 to set-up baseband input signal routing as described in Table 3-4.
9	BASEBAND INPUT CHAN 3 J3	Connector, enables baseband input for demodulator unit 3.
10	BRDG S2 BRDG/INDEP	Two position switch, used with switches S1 and S3 to set-up baseband input signal routing as described in Table 3-4.
11	BASEBAND OUTPUT J5	Connector, enables additional demodulation, with proper switching, of CHAN 1 J1 or CHAN 2 J2 inputs.
12	BASEBAND INPUT CHAN 2 J2	Connector, enables baseband input for demodulator unit 2.
13	BRDG S1 BRDG/INDEP	Two position switch, used with switches S2 and S3 to set-up baseband signal routing as described in Table 3-4.
14	BASEBAND INPUT CHAN 1 J1	Connector, enables baseband input for demodulator unit 1.

Table 2-1. Control Rack Frame Rear Panel Connections and Controls (Concluded)

Index No.	Panel Nomenclature	Function/Description
15	AUDIO OUTPUT J3	Connector, enables demultiplexed audio output from Demodulator.
16	REF IN J1	Connector, enables input of nominal 1 MHz external frequency standard.
17	F1 1.5 AMP SLOW BLOW	Fuse and fuse holder, protects demodulator with line select switch S1 in 115 V position.
18	115 V S2 230 V	Two position switch, enables selection of either 115 Vac or 230 Vac as input power.
19	F2 0.75 AMP SLOW BLOW	Fuse and fuse holder, protects demodulator with line select switch S1 in 230 V position.
20	GND	Connection, provides chassis ground.
21	POWER 115/230 VAC	Connector, provides power input.

2.7 PREPARATION FOR USE

CAUTION

To prevent possible damage to the Demodulator, make sure the equipment power switches are off, Line Voltage Select switch S2 (on control rack frame rear panel) is set for proper line voltage, and facility power to Demodulator is off.

NOTE

The following procedures are strictly preparation for first use procedures and are NOT pre-operation or turn-on procedures.

1. Verify or set Line Voltage Select switch S2 in desired position.
2. Verify or set Demodulator power switch in off (down) position.
3. Verify that fuses F1 (1.5 amp, slow-blow) and F2 (0.75 amp, slow-blow) are installed.
4. Perform Demodulator cable interconnection to desired configuration.
5. Verify or establish correct Demodulator address by performing procedures in paragraph 2.7.1.
6. Connect Demodulator power cable from demodulator power connector FL1J1 to facility power.
7. If power is off, turn on facility to Demodulator power.

2.7.1 ESTABLISH DEMODULATOR ADDRESS

Establish, or verify, correct Demodulator address by performing the following procedures.

1. Loosen two captive screws securing control unit to control rack frame and remove control unit.
2. Remove cover from control unit.
3. Remove IEEE 488/RS 232 I/O Assembly (A1A3) and establish, or verify, correct Demodulator address on device address dip switch A3S3 using Table 2-2.
4. Reinstall IEEE 488/RS 232 I/O Assembly (A1A3) in control unit.
5. Reinstall cover on control unit.
6. Reinstall control unit in control rack frame and secure using two captive screws.

Table 2-2. Switch (A3S3) to Address Settings

Address (Decimal)	Switch (A3S3) Settings							
	1	2	3	4	5	6	7	8
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
03	0	0	0	0	0	0	1	1
04	0	0	0	0	0	1	0	0
05	0	0	0	0	0	1	0	1
06	0	0	0	0	0	1	1	0
07	0	0	0	0	0	1	1	1

Table 2-2. Switch (A3S3) to Address Settings (Continued)

Address (Decimal)	Switch (A3S3) Settings							
	1	2	3	4	5	6	7	8
08	0	0	0	0	1	0	0	0
09	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
15	0	0	0	0	1	1	1	1
16	1	0	0	0	0	0	0	0
17	1	0	0	0	0	0	0	1
18	1	0	0	0	0	0	1	0
19	1	0	0	0	0	0	1	1
20	1	0	0	0	0	1	0	0
21	1	0	0	0	0	1	0	1
22	1	0	0	0	0	1	1	0
23	1	0	0	0	0	1	1	1
24	1	0	0	0	1	0	0	0
25	1	0	0	0	1	0	0	1
26	1	0	0	0	1	0	1	0
27	1	0	0	0	1	0	1	1
28	1	0	0	0	1	1	0	0
29	1	0	0	0	1	1	0	1
30	1	0	0	0	1	1	1	0
31	1	0	0	0	1	1	1	1
32	0	1	0	0	0	0	0	0

0 = switch in CLOSED position.
1 = switch in OPEN position.

2.8 PREPARATION FOR STORAGE OR SHIPMENT

2.8.1 ENVIRONMENT

The equipment should be stored in a clean, dry environment. The following environmental conditions apply to both storage and shipment of the Demodulator:

1. Maximum humidity: 95% (with no condensation)

2. Temperature range: -30°C to 85°C (-53°F to 185°F)

2.8.2 PACKAGING

2.8.2.1 Original Packaging

If retained, the original packaging materials can be used for packaging the Demodulator for storage or shipment.

2.8.2.2 Other Packaging

Package the Demodulator for storage or shipment using packaging methods which follow the pattern established in the original shipment or use local established procedures for packaging of electronic equipment.

SECTION III

OPERATION

3.1 GENERAL

This section contains an explanation of the use and function of each control and indicator of the control rack frame, control unit, and demodulator unit. It also contains the initial start-up and operation procedures, normal start-up and operation procedures, and operator maintenance.

3.2 CONTROLS AND INDICATORS

3.2.1 CONTROL RACK FRAME

Control rack frame front panel controls and indicators are illustrated in Figure 3-1 and described in Table 3-1.

3.2.2 CONTROL UNIT

Control unit front panel controls are illustrated in Figure 3-2 and described in Table 3-2.

3.2.3 DEMODULATOR UNIT

Demodulator unit front panel indicators are illustrated in Figure 3-3 and described in Table 3-3.

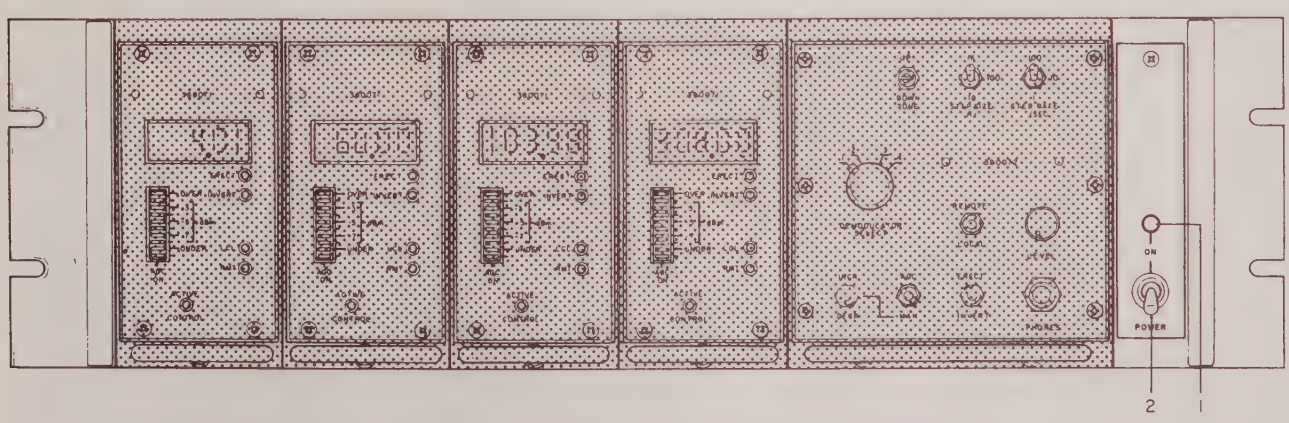


Figure 3-1. Control Rack Frame Front Panel

Table 3-1. Control Rack Frame Front Panel Controls and Indicators

Index No.	Panel Nomenclature	Function/Description
1	None	Indicator, lights to indicate power is applied to demodulator.
2	ON/POWER	Two position toggle switch, enables application of power to demodulator.

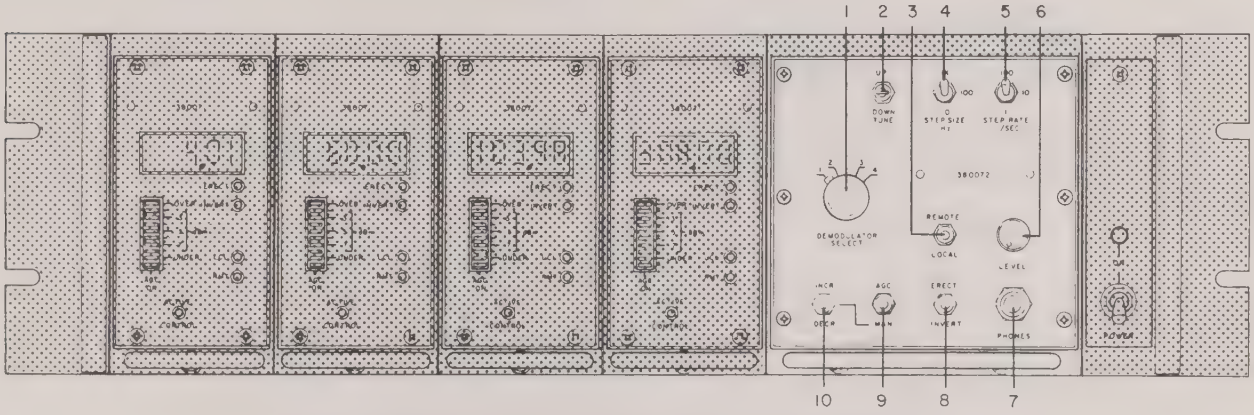


Figure 3-2. Control Unit Front Panel

Table 3-2. Control Unit Front Panel Controls

Index No.	Panel Nomenclature	Function/Description
1	DEMODULATOR SELECT	Four position rotary switch, provides selection of demodulator unit to be monitored or set.
2	UP/DOWN TUNE	Momentary contact switch, provides up/down tuning of selected demodulator in conjunction with STEP SIZE and STEP RATE switches.
3	REMOTE/LOCAL	Momentary contact switch provides local change of status of selected demodulator unit from remote to local.
4	STEP SIZE, Hz	Three position switch, provides selection of frequency step sizes of 10 Hz, 100 Hz, and 1 kHz.

Table 3-2. Control Unit Front Panel Controls (Concluded)

Index No.	Panel Nomenclature	Function/Description
5	STEP RATE/SEC	Three position switch, provides selection of step rates of 1, 10, 100 steps per second.
6	LEVEL	Control, provides adjustment of level of volume of audio output via phones jack.
7	PHONES	Headphones jack, provides phone access to audio output.
8	ERECT/INVERT	Momentary contact switch, provides selection of mode of single sideband of selected frequency.
9	AGC/MAN	Momentary contact switch, provides selection of either automatic gain control or manual gain control with manual gain control selection necessary for use of INCR/DECR switch.
10	INCR/DECR	Momentary contact switch, provides increase or decrease of demodulator unit gain (at the rate selected by the STEP RATE/SEC switch) when manual gain control mode is selected.

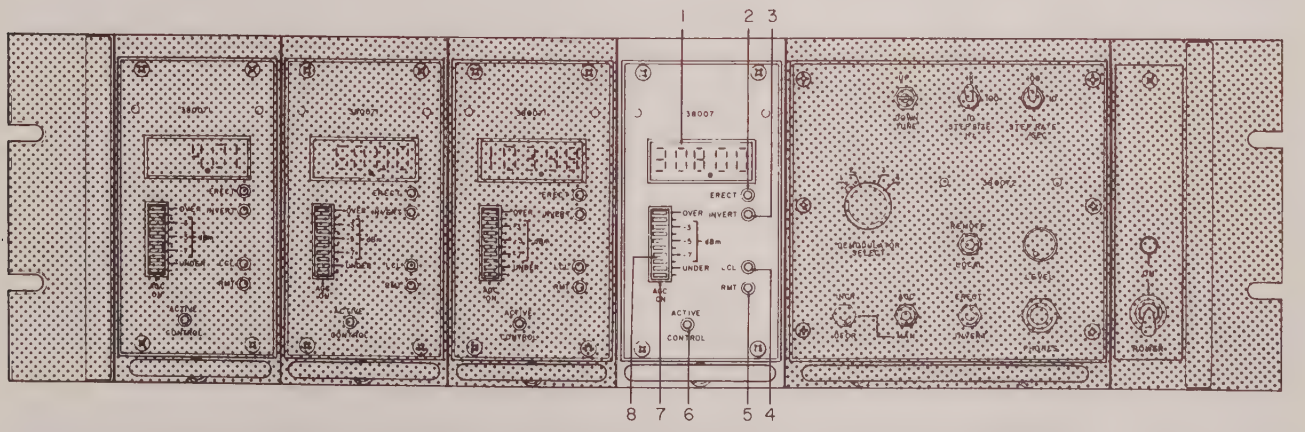


Figure 3-3. Demodulator Unit Front Panel

Table 3-3. Demodulator Unit Front Panel Controls and Indicators

Index No.	Panel Nomenclature	Function/Description
1	None	5-digit numeric display, indicates current demodulator unit's tuned frequency in kHz.
2	ERECT	Indicator lamp, when lighted indicates that the erect single sideband is selected.
3	INVERT	Indicator lamp, when lighted indicates that the inverted single sideband is selected.
4	LCL	Indicator lamp, when lighted indicates that the demodulator unit is under local control from the control unit panel.
5	RMT	Indicator lamp, when lighted indicates that the demodulator unit is under remote (other than local) control.
6	ACTIVE CONTROL	Indicator lamp, when lighted indicates that the demodulator unit has been selected by either the control unit or remote controller.
7	AGC ON	Indicator lamp, when lighted indicates that the automatic gain control function of the demodulator unit is active.
8	dBm OVER UNDER	Indicator lamps, indicate the output level in either AGC or MAN mode. Indications are from -2 to -8 dBm with OVER (more than -2) and UNDER (less than -8) out-of-range indication.

3.3 BASEBAND SIGNAL DISTRIBUTION AMPLIFIER ASSEMBLY A1A1

The baseband signal distribution amplifier assembly, located in the upper right quadrant of the control rack frame rear panel as illustrated in Figure 1-3 and described in Table 2-1, provides the capability of switching the various input channels to selected demodulator units and baseband output connectors. Table 3-4 lists the input channel to switch position

to output relationships for the baseband signal distribution amplifier. In addition to setting up desired baseband input signal routing, it may be used as part of the initial start-up and operation procedures in paragraph 3.4 to verify the operating integrity of the Demodulator.

Table 3-4. Baseband Input Channel to Output Switching

Input To Channel Jack No.	Switch Position			Input To				Output To	
	S1	S2	S3	DEMOD 1	DEMOD 2	DEMOD 3	DEMOD 4	J5	J6
1	BRDG	INDEP	INDEP	X*	X	-	-	X	-
1	INDEP	INDEP	INDEP	X	-	-	-	-	-
1	BRDG	BRDG	INDEP	X	X	X	-	X	-
1	BRDG	BRDG	BRDG	X	X	X	X	X	X
2	BRDG	ANY	ANY	-	-	-	-	-	-
2	INDEP	INDEP	INDEP	-	X	-	-	X	-
2	INDEP	BRDG	INDEP	-	X	X	-	X	-
2	INDEP	BRDG	BRDG	-	X	X	X	X	X
3	ANY	BRDG	INDEP	-	-	-	-	-	-
3	ANY	INDEP	INDEP	-	-	X	-	-	-
3	ANY	INDEP	BRDG	-	-	X	X	-	X
4	ANY	ANY	BRDG	-	-	-	-	-	-
4	ANY	ANY	INDEP	-	-	-	X	-	X

NOTE

* X denotes output available when switches are in positions indicated with input to respective CHAN input.

3.4 INITIAL START-UP AND OPERATION

The following initial start-up and operation procedures are provided to ensure the integrity of the Demodulator assemblies and installation. The procedures validate correct operation of the control unit and associated demodulator units in the local mode of operation.

1. Set POWER switch to ON. Power on lamp lights. All digits are displayed on all carrier kHz displays.

2. Set DEMODULATOR SELECT switch to 1. Demodulator unit 1 ACTIVE CONTROL and LOCAL lamps light. Demodulator unit ERECT or INVERT lamp lights.

3. Press ERECT/INVERT switch. ERECT lamp turns off and INVERT lamp lights or ERECT lamp lights and INVERT lamp turns off.

4. Set control unit STEP SIZE switch to 10 and STEP RATE/SEC to 1 and hold TUNE switch in UP position. Demodulator unit carrier, kHz display advances at a rate of 10 Hz/sec. Release TUNE switch.

5. Set STEP SIZE switch to 100 and STEP RATE/SEC to 10 and hold TUNE switch in UP position. Carrier, kHz display advances at a rate of 1000 Hz/sec. Release TUNE switch.

6. Set STEP SIZE switch to 1K and STEP RATE/SEC to 100 and hold TUNE switch in UP position. Carrier, kHz display advances at a rate of 100 kHz/sec. Release TUNE switch.

7. Rotate LEVEL control counterclockwise and plug in headphones in PHONES jack.

8. Using STEP SIZE Hz, STEP RATE/SEC and TUNE switches while observing the carrier, kHz display, adjust active demodulator unit for known frequency.

9. If necessary, set AGC MAN switch to MAN position. Demodulator unit AGC lamp goes out.

10. Using INCR-DECR switch while observing demodulator unit OUTPUT LEVEL dBm indicators, adjust output level to -5 dBm.

11. Adjust LEVEL control for a comfortable listening level.

12. Using STEP SIZE Hz, STEP RATE/SEC and TUNE switches while observing the carrier, kHz display, adjust active demodulator unit for a frequency of 000.00.

13. Using procedures in steps 2 through 12, as necessary, verify performance of remaining demodulator units.

14. Set POWER switch to OFF.

3.5 START-UP OPERATION

The following start-up and operation procedures are provided as a non-specific general procedure as a result of the varied anticipated operating conditions.

NOTE

The following procedures are based on a Local Control Mode.

1. Set POWER switch to ON.

2. Set DEMODULATOR SELECT switch to desired demodulator unit number.

3. Set ERECT/INVERT switch to desired condition (as observed on selected demodulator unit).

4. Rotate LEVEL control counterclockwise, plug in headphones in PHONES jack, and adjust LEVEL control for a comfortable listening level.

5. Using STEP SIZE, STEP RATE/SEC and TUNE switches either adjust selected demodulator unit to desired frequency or scan.

6. If necessary, adjust gain by pressing AGC/MAN switch and adjusting gain using INCR DECR switch.

7. Enable and set-up remaining demodulator units, as required, using procedures in steps 2 through 6.

3.6 LOCAL SELECTION OF A DEMODULATOR UNIT

Selection of a remote demodulator unit for local use is accomplished by performing the following procedures. The procedures assume that the demodulator is fully operational and has a remote interface and operating remote controller. It is also assumed that at least one demodulator unit is operating in the remote mode.

1. Set DEMODULATOR SELECT switch to desired demodulator unit operating in remote mode.

2. Press and release REMOTE/LOCAL switch. Change of control of selected demodulator unit is indicated by RMT lamp going out and LCL lamp lighting.

3.7 REMOTE PROGRAMMING INFORMATION

Remote programming of the Demodulator is accomplished with a bi-directional bus, via the 24-pin REMOTE CONTROL IEEE 488 connector J2 on the rear panel of the control rack frame. Associated with connector J2 is instrument address switch S3, located on IEEE-488/RS-232 I/O Assembly A2A1A3, which is used to establish the Demodulator address. The Demodulator can be addressed to send output data (TALK) or accept program information (LISTEN). Several of the IEEE-488 terms are defined as follows:

1. A TALKER sends information to the CONTROLLER, REMOTE CONTROLLER, via the bi-directional bus.

2. A LISTENER receives information from the CONTROLLER, REMOTE CONTROLLER, via the bi-directional bus.

3. A CONTROLLER, REMOTE CONTROLLER, is the instrument, or device, which manages the instruments (Demodulators) connected to the bi-directional bus. It addresses other instruments connected to the bi-directional bus as TALKERS or as LISTENERS. It is a TALKER and may be a LISTENER.

4. A HIGH or 0 level of a line or switch is the more positive signal level (≧2.4 Vdc) while a low or 1 level is the less positive signal level (≧0.4 Vdc).

3.7.1 BI-DIRECTIONAL BUS

The bi-directional bus is a 15-line bus consisting of 8 data lines, 3 transfer lines, and 4 control and status lines. The data lines are described in paragraph 3.7.1.1; the transfer lines in paragraph 3.7.1.2; and the control and status lines in paragraph 3.7.1.3.

More than one Demodulator can be connected to the bi-directional bus. The number of Demodulators depends on the drive capability of the controller. A specific Demodulator is made to send output data (TALK) or accept program data (LISTEN) by addressing it to do so. The procedure for establishing a unique Demodulator address is described in paragraph 2.7.

3.7.1.1 Data Lines

Data lines DI01 through DI08 provide the means of communicating addresses, program, and output information from one device to another on the bi-directional bus. The Demodulator drives these lines when it has been addressed to TALK by the controller. It receives information on the data lines when control and status line ATN, described in paragraph 3.7.1.3, is low and it has been addressed to LISTEN by the controller.

Message bytes on the data lines are in byte-serial, bit-parallel form. When a data line is high, the data bit is a logic zero and conversely, when a data line is low, the data bit is a logic one.

3.7.1.2 Transfer Lines

The three transfer lines, or interface signal lines, are NRFD (not ready for data), NDAC (not data accepted), and DAV (data valid). The transfer lines are used to effect the transfer of each byte of data on the data lines from a talker, or controller, to one or more listeners. They must interact in the proper time sequence before complete communication between devices is established.

3.7.1.2.1 NRFD

NRFD is the transfer line that indicates listeners are ready to accept information on the data lines. Its relationship to NDAC and DAV transfer lines and the ATN control line is shown in Figure 3-4 and Table 3-5. It is driven by all listeners when ATN is low and, those devices addressed to listen when ATN is high.

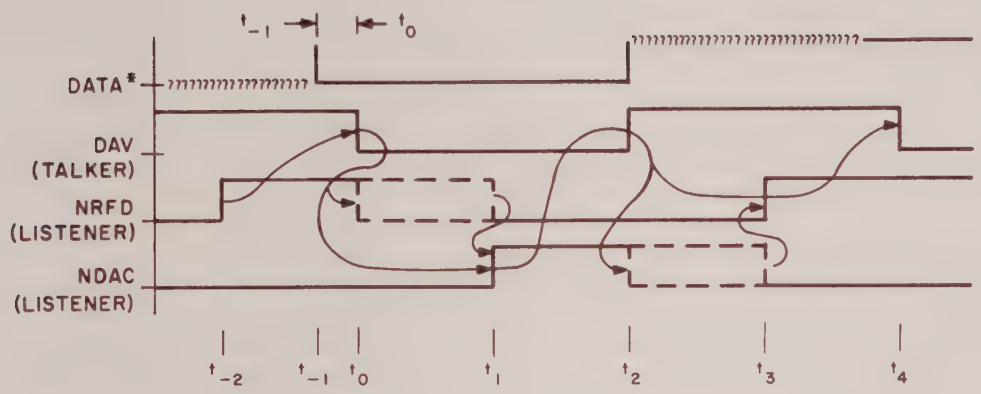
When NRFD is high, all listeners are unconditionally ready for data. The talker may, at this time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more listeners are not ready to accept data.

When the controller sets ATN low, all Demodulators set NRFD high within 200 ns. When it sets ATN high, all Demodulators not addressed to listen will not drive NRFD.

The listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets NDAC high. It must not return NRFD high until it senses DAV is high and may do so before or at the same time it sets NDAC low.

3.7.1.2.2 NDAC

NDAC is the transfer line that indicates the acceptance of information on the data lines. It is driven by all listeners when ATN is low and, those devices addressed to listen when ATN is high.



EVENTS

t_{-2}	:	LISTENER BECOMES READY TO ACCEPT DATA.
t_{-1}	:	TALKER HAS PUT DATA ON THE LINES.
t_0	:	INDICATES DATA IS VALID.
t_1	:	LISTENER HAS ACCEPTED THE DATA AND NO LONGER REQUIRES IT HELD VALID.
t_2	:	TALKER INDICATES THE DATA IS NO LONGER VALID AND MAY CHANGE IT.
t_3	:	LISTENER INDICATES IT IS READY FOR NEW DATA.
t_4	:	A NEW CYCLE BEGINS (EQUIVALENT TO t_0).
t_{-1} TO t_0	:	TIME THAT DATA IS PUT ON LINES BEFORE DAV IS SET LOW.

*A COMPOSITE OF THE DIO1 THROUGH DIO7 LINES FOR ILLUSTRATIVE PURPOSES.
(THE CURVED LINES INDICATE INTERLOCKED SIGNAL SEQUENCE)

Figure 3-4. Transfer Lines Timing

Table 3-5. Relationship of ATN Line and Transfer Lines

	NRFD		NDAC		DAV	
	LOW	HIGH	LOW	HIGH	LOW	HIGH
† Attention (ATN) Line State	† Address Mode LOW					
	One or more Demodulator not ready for data	All Demodulators are ready for data	One or more Demodulator has not accepted the data	All Demodulators have accepted the data	Controller has valid data on lines	Controller data not valid
	(1) Driven by all demodulators (2) Sensed by controller				(1) Driven by controller (2) Sensed by demodulators	
	† Address Mode HIGH					
	One or more listeners are not ready for data	All addressed listeners are ready for data	One or more listeners have not accepted data	All addressed listeners have accepted the data	The addressed talker has valid data on lines	The addressed talker's data not valid
	(1) Driven by all devices addressed to LISTEN (2) Sensed by the device addressed to TALK (3) All devices not addressed will not drive				(1) Driven by the devices addressed to TALK (2) Sensed by all devices addressed to LISTEN	

When NDAC is high, all listeners have unconditionally accepted the byte of information on the data lines and no longer need it. The talker may, at this time, set DAV high, remove the byte of information, and continue. When NDAC is low, one or more listeners have not accepted the information on the data lines.

3.7.1.2.3 DAV

DAV is the transfer line that indicates that an ASCII character is already on the data lines. It is driven by talkers only.

When DAV is low, the states of the data lines are unconditionally valid and may be accepted by all listeners at their own time. DAV can be driven low only if NRFD is high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

3.7.1.3 Control and Status Lines

Only two of the four control and status lines, ATN (attention) and SRQ (service request), are used with the Demodulator. The remaining two control and status lines, REN (remote enable) and IFC (interface clear), are dead-ended in this application. ATN and SRQ are used to supervise and control an orderly flow of information across the interface.

3.7.1.3.1 ATN

ATN is the control line used by a controller to address a Demodulator, which monitors ATN at all times.

When ATN is low, all Demodulators connected to the bi-directional bus interpret the information on the data lines as an address. When ATN is high, the Demodulator that has been addressed to talk will drive the data lines. The Demodulators that have been addressed to listen will interpret the information on the data lines as data. Those that have not been addressed will not drive the data lines.

3.7.1.3.2 SRQ

SRQ is the status line used by a Demodulator to perform two functions with respect to the controller, or remote controller. The first is at Demodulator "power-up" and may be used, in serial poll format, to indicate to the controller that a bus-attached Demodulator has just powered-up and is available for remote control.

SRQ is cleared (0 to 1) when a serial poll-to-device address is completed, giving the controller the "on-line" response. No "selected demod" is sent with the status byte, and the controller recognizes this as a "power-up" rather than a Remote-to-Local request as described in the following paragraph.

The second function is to flag the controller when a Remote-to-Local operator request is initialized via the control unit REMOTE/LOCAL switch. The demodulator unit selected via the control unit DEMODULATOR SELECT switch is placed in the local mode upon operation of the REMOTE/LOCAL switch. At the same time SRQ is set true. As a result, the controller may interpret which demodulator unit changed remote/local status by using the serial poll technique.

3.7.2 DATA TRANSFER

Data transfer on the bus is asynchronous and places no restrictions on the data rates of devices connected to the bus. The transfer of each byte of data on the data lines is under the control of the NRFD, NDAC, and DAV transfer lines described in paragraph 3.7.1.2. The timing and levels required to transfer a byte of data are shown in Figure 3-4.

The transfer of a byte is initiated by the listener by setting NRFD high, signifying it is ready for data. When the talker recognizes NRFD is high, it places valid data on the data lines and sets DAV low. The listener, in turn, senses that DAV is low and accepts the data. After using the data, the listener sets NDAC high. Since all the devices on the bus have their corresponding lines connected in parallel, all listeners must be in a high state before any particular line, as NRFD, goes high. This wire-AND situation allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

3.7.3 PROGRAMMING CODES

The Demodulator operates in response to a specific set of programming codes. These codes, listed in Table 3-6, determine the configuration of the Demodulator in the remote mode of operation. All front panel control functions, with the exceptions of the STEP SIZE and STEP RATE functions, can be remotely programmed. Frequency and gain slew functions must be implemented as part of the remote controller. The Demodulator also responds to a set of special action codes. These codes, listed in Table 3-7, determine the operating state of the Demodulator. A sample program utilizing both sets of codes is listed in Table 3-8.

Table 3-6. Programming Codes

DIO 7 6 5 4 3 2 1	ASCII Equivalent	Demodulator Response
1 0 0 0 0 1 0 0 (ASCII code form)	Dn (with n = 0, 1, 2, 3 as second byte)	This code specifies the demodulator unit to be controlled. Subsequent commands may be sent any number of times without repeating this code (e.g., frequency stepping).
1 0 0 1 1 0 0	L	Sets the specified demodulator unit to the local mode. NOTE - Two demodulator units within a given Demodulator may be simultaneously in the local or remote mode.
1 0 1 0 0 1 0	R	Sets the specified demodulator unit to the remote mode.
1 0 0 0 1 1 0	Fxxxxx	Sets the selected demodulator unit to the frequency "xxxxx". Frequency must be between 00000 and 30800 (000.000 kHz to 308.000 kHz). NOTE - Do not send a decimal.
1 0 0 0 1 0 1	E	Sets the selected demodulator unit to the erect signal mode.
1 0 0 1 0 0 1	I	Sets the selected demodulator unit to the invert signal mode.
1 0 0 0 0 0 1	A	Sets the selected demodulator unit to the AGC mode.
1 0 0 0 1 1 1 0 1 0 1 0 1 1	G+	In manual gain mode, increases the gain of the selected demodulator unit by one step. In AGC mode, the first command puts demodulator unit in the manual gain mode and increases gain.
1 0 0 0 1 1 1 0 1 0 1 1 0 1	G-	In manual gain mode, decreases the gain of the selected demodulator unit by one step. In AGC mode, the first command puts demodulator unit in the manual gain mode and decreases gain.

Table 3-7. Special Action Codes, Universal Commands

Command	ASCII Character	Octal Code	Purpose
SPE-Serial Poll Enable	CAN	030	Enables serial poll mode on bus
SPD-Serial Poll Disable	EM	031	Disables serial poll mode on bus

Table 3-8. Programming Examples

Funtion	Control Lines REN	Control Lines ATN	DIO Lines ASCII Code	Equivalent 9825 Command	Description of Program Sequence
Set A Parameter	L	L	?	wrt 703, "E"	UNL (Unlisten)
	L	L	U		MTA (Talk address of controller)
	L	L	#		MLA (Listen address of Demodulator)
	L	H	E		ASCII data to be sent
	L	H	CR		Carriage return
	L	H	LF		Line feed
Read Status	L	L	?	red 703, B $	UNL (Unlisten)
	L	L	5		MLA (Listen address of controller)
	L	L	C		MTA (Talk address of Demodulator)
	L	H	Dxxxxxxxxxxxxx		14 character ASCII string representing demodulator unit status
	L	H	CR		Carriage return
	L	H	LF		Line feed

NOTE

See IEEE STANDARD 488-1978 for:

1. 488 Connector specifications (Section 4), and
2. 488 Bus Handshake timing (Appendix B).

3.7.4 BASIC CONTROL FUNCTIONS FROM A 9825 CONTROLLER

All data transfers from the 9825 Controller to the Demodulator are accomplished by "red" or "wrt" statements. The serial poll function uses the "rds", read status command, returning numerical data to a 9825 register. The demodulator will respond to only "legal"

ASCII strings as defined in the following paragraphs. Operator entries are enclosed in single quotes (" "), and 9825 display data are in double quotes (" " " ").

3.7.5 AVAILABLE FUNCTIONS

The available functions are:

1. Demodulator status display,
2. remote-local select,
3. erect-invert select,
4. AGC-manual gain (adjustable),
5. direct set frequency,
6. frequency slew (rate limited by 9825; step size by selection), and
7. remote-local change request from the demodulator by interrupt response.

3.7.6 DEMODULATOR SELECT

"wrt 703," "Dn" " " (with n as demodulator number; D_0 = DU1, D_1 = DU2, D_2 = DU3, D_3 = DU4).

NOTE

Since this command asserts the demodulator to be controlled, it must be the first command executed.

3.7.7 SET MODES, ERE-INV, REM-LOC, AGC-MAN

"wrt 703, " "X" " " (with *X = 1st letter. E, I, R, L, A, or G+ or G-).

3.7.8 SET FREQUENCY

"wrt 703, " "Fnnnnn" " "

NOTE

Five digits must be supplied without a decimal.

3.7.9 READ DEMODULATOR STATUS

"red 703, A $ "

NOTE

1. The string "A$" must be previously dimensioned. This loads the demodulator status into the string and allows display with the "dsp A$" instruction when executed by the operator.

2. In order to follow the changing status of a locally operated demodulator, a "wrt 703, " "Dn" " " must precede each "red" command to prompt an " "ASCII" " routing update for that demodulator.

3.7.10 READ BUS STATUS (SERVICE REQUEST)

"rds (703) A; dsp A"

The bus status is displayed as 65 through 79 if any demodulators have been requested locally. With the service request byte written as 0100XXXX and the four least significant digits representing D_3, D_2, D_1, D_0 (DU4, DU3, DU2, DU1, respectively); the bus status, when displayed as 65, signifies that demodulator unit one has changed status from remote to local. A 66 signifies demodulator unit two, and so on to a 79, which signifies all demodulator units. The service request response automatically clears the service request line.

3.8 SHUT DOWN AND INTERRUPTED POWER

During shut down or an interrupted power situation, the Demodulator's programmed memory will be kept alive for a time span of approximately 72 hours by internal backup batteries. After backup battery discharge, all memory, consisting of demodulator addresses and frequencies, is lost and must be reprogrammed.

SECTION IV
THEORY OF OPERATION

4.1 GENERAL

This section contains the theory of operation of the Demodulator and its subordinate assemblies. Since all four demodulator units, A3, A4, A5, and A6, are identical to each other, the theory of operation of only one, A3, is described.

4.2 OVERALL FUNCTIONAL DESCRIPTION

Baseband input signals, from 200 Hz to 308 kHz, are input at connectors J1 through J4, CHAN 1 through CHAN 4, respectively, to the baseband signal distribution amplifier (Figure 4-1) which amplifies baseband inputs by 6 dB, reduces the 93 Ω input impedance to 14 Ω, and provides the capability of switching the various input channels to selected demodulator units and baseband output connectors. As illustrated in Figure 4-1, the CHAN 1 input is applied to demodulator unit A3, CHAN 2 is applied to demodulator unit A4 and baseband output connector J5, CHAN 3 is applied to demodulator unit A5, and CHAN 4 is applied to demodulator A6 and baseband output connector J6.

The 1 MHz reference input signal at connector J1 is applied to the reference generator assembly which converts the reference input signal into a 2 MHz signal for use by the demodulator units. In case of the absence of the 1 MHz reference input signal, the reference generator switches to an internal 2 MHz source for use by the demodulator units.

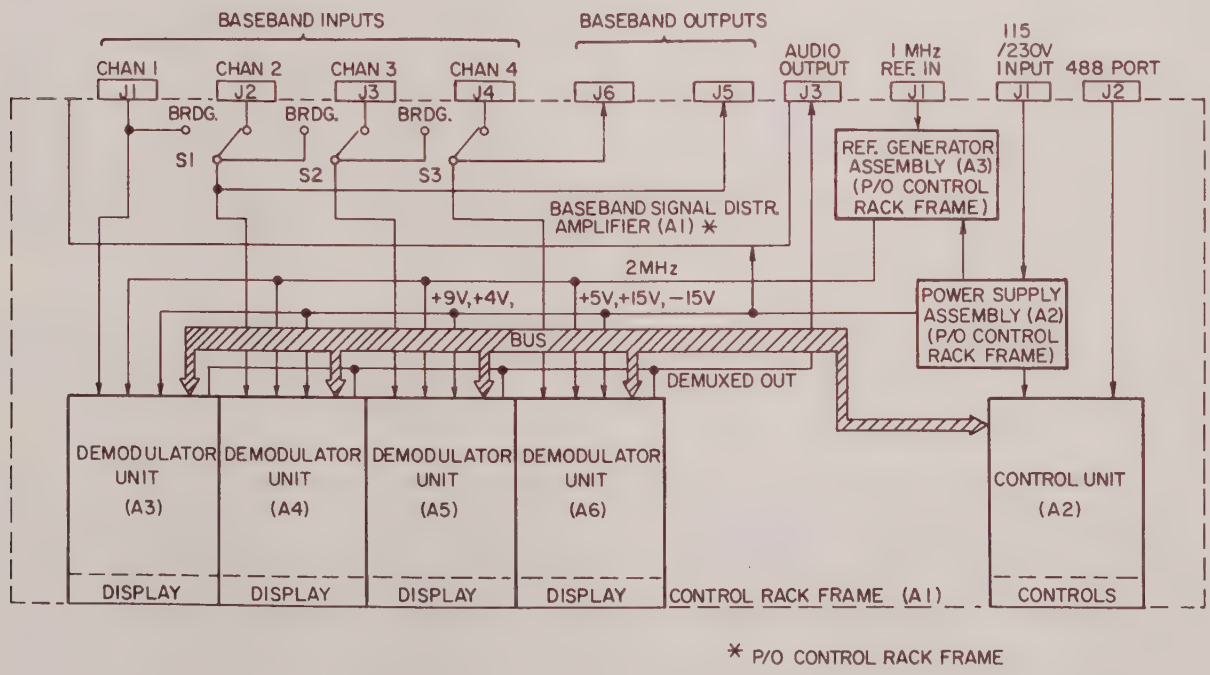


Figure 4-1. Demodulator Functional Block Diagram

The 115 Vac or 230 Vac power input, selected via switch S2 (Figure 4-4) on the rear panel of the control rack frame, is input to the power supply assembly via connector J1 and power transformer T1 on the control rack frame. Transformer T1 provides a nominal 18.8 Vac and a center-tapped ground potential to the power supply assembly. The power supply assembly, in turn, provides a +8 volt unregulated output, a +9 volt unregulated output to voltage regulators VR1 and VR2, a +20 and -20 volt unregulated output to voltage regulators VR3 and VR4, and a +4 volt unregulated output. Voltage regulator VR1, supplies regulated +5 Vdc to the control unit digital circuits, VR2 supplies regulated +5 Vdc to the demodulator unit digital circuits, VR3 and VR4 supply regulated +15 and -15 Vdc for use by the Demodulator, and the +4 volt unregulated output is used to drive the demodulator unit LED displays.

The control unit consists of front panel mounted controls and indicators, three printed-circuit boards plugged into a motherboard, and interface connections. It provides the means of selection, tuning, and control of the demodulator units in either a local or remote mode. The selection, tuning, and control functions are performed by the control unit digital hardware and associated software routine via an 8-bit bi-directional data bus to each of the four demodulator units. Interface with the IEEE-488 Bus is provided to the Demodulator via connector J2 on the rear panel of the control rack frame.

Selection, tuning, and control functions via the control unit front panel are input to the panel interface and demodulator control assembly which modifies, or translates, the front panel input data and interfaces the data to and from the microprocessor on the CPU processor and memory assembly. Inputs via the IEEE Bus are applied to the IEEE-488/RS-232 I/O assembly which contains an MC68488 general purpose interface adapter and necessary external logic to establish data flow to and from the microprocessor on the CPU processor and memory assembly.

Baseband signal inputs, from 200 Hz to 308 kHz, from the baseband signal distribution amplifier are input to and processed by the input converter assembly to produce a 2.0 MHz IF output and an analog output. The 2.0 MHz IF output is filtered by filter FL1 and applied to the IF demodulator assembly which mixes the filtered output from FL1 with the 2 MHz input signal from the 2 MHz reference buffer on the demodulator unit motherboard. The resultant audio signal is fed to audio output connector J3 on the control rack frame rear panel and to the attenuator control assembly where, when enabled by the insertion of a phones jack, is made available at the control unit front panel.

The analog output from the input converter assembly is used to select the level of attenuation placed on the baseband signal input path. The 2 MHz signal from the reference generator assembly, in addition to being fed to the IF demodulator, is also applied to the coarse loop of the LO synthesizer to provide the fixed reference input for coarse loop operation.

Setting or changing the control unit front panel frequency-related controls results in an established or changed output from the microprocessor to the LO synthesizer of the selected demodulator unit via the data bus, or data stream. The frequency data bits are input to the loops of the LO synthesizer to provide a predetermined variable which is compared against fixed reference inputs to establish or change the LO frequency of the demodulator unit.

Inputs to the selected demodulator unit control register from the control unit are displayed on the demodulator unit front panel.

4.3 CONTROL RACK FRAME (A1)

4.3.1 FUNCTIONAL DESCRIPTION

The control rack frame, Figure 7-1, in addition to providing mechanical support and electrical interfacing for the control unit and demodulator units, contains Baseband Signal Distribution Amplifier Assembly A1A1, Power Supply Assembly A1A2, and Reference Generator Assembly A1A3.

4.3.2 TYPE 796074 BASEBAND SIGNAL DISTRIBUTION AMPLIFIER ASSEMBLY (A1A1)

The baseband signal distribution amplifier assembly consists of Baseband Signal Distribution Amplifier PC Assemblies A1A1A1 and A1A1A2, switches S1, S2, and S3, input connectors J1 through J4, internal output connectors J7 through J9, and external output connectors J5, J6. It amplifies baseband inputs by 6 dB, reduces the 93 Ω input impedance to 14 Ω, and provides the capability of switching the various input channels to selected demodulator units and baseband output connectors.

Refer to Figure 4-2 for the block diagram and Figure 7-2 for the schematic diagram of Baseband Signal Distribution Amplifier Assembly A1A1. Baseband inputs for the Demodulator are via CHAN 1 through CHAN 4 input jacks J1 through J4, respectively, of the baseband signal distribution amplifier on the rear panel of the Demodulator. Each of the four inputs is buffered by an independent emitter-follower buffer. The output of the CHAN 1 buffer is applied to an additional amplifier-buffer which drives DEMUX 1 output J7. The output of the CHAN 1 buffer is also wired to the BRDG contact of switch S1. The output of the CHAN 2 buffer is wired to the $\overline{\text{BRDG}}$ contact of switch S1. As a result, this allows switch S1 to be used to select either the CHAN 1 buffered output to be routed to DEMOD 1 connector J7 when in the $\overline{\text{BRDG}}$ position while allowing the CHAN 2 buffered output to be routed to DEMOD 2 and BASEBAND OUT 1 connectors J8 and J5, respectively, or the CHAN 1 buffered output to be routed to DEMOD 2 and BASEBAND OUT 1 connectors when in the BRDG position.

The CHAN 2 amplifier-buffers are wired in parallel at E13. Quad amplifier U4 is identical to U2 which drives the DEMOD 1 output. The other drives a 93 Ω baseband load. Input/output relationships for switches S1, S2, and S3 are described in Table 3-4.

4.3.2.1 Type 796065 Baseband Signal Distribution Amplifier PC Assemblies (A1A1A1 and A1A1A2)

Refer to Figure 4-3 for the block diagram and Figure 7-3 for the schematic diagram of Baseband Signal Distribution Amplifier PC Assemblies A1A1A1 and A1A1A2. Input amplifier buffer U1 is a quad transistor wired as a complementary emitter-follower. U1 and quad amplifier U3 are identical in function and performance. As a result, the description for U1 applies for U3.

Resistor R1 terminates the input signals for CHAN 1 and CHAN 3 inputs. This input signal is applied to the emitters of U1B and U1C. The base and collector of U1B and U1C are wired together with the result that U1B and U1C function as diodes with each collector-base combination operating at the same potential.

U1A and U1D are wired as complementary emitter-followers; one driving the other. The DC biasing for U1A and U1D is provided by U1B and U1C, and resistors R2 and R8. U1A and U1D provide a very low source impedance for the voltage impressed on E6, which, on PC assembly A1A1A1 (CHAN 1 input), is wired directly to E7, providing a signal path to the

DEMUX 1 output. For CHAN 2 through CHAN 4 inputs, E6 is wired to the independent (INDEP) side of the associated switch as illustrated in the block diagram for the Baseband Signal Distribution Amplifier, Figure 4-2.

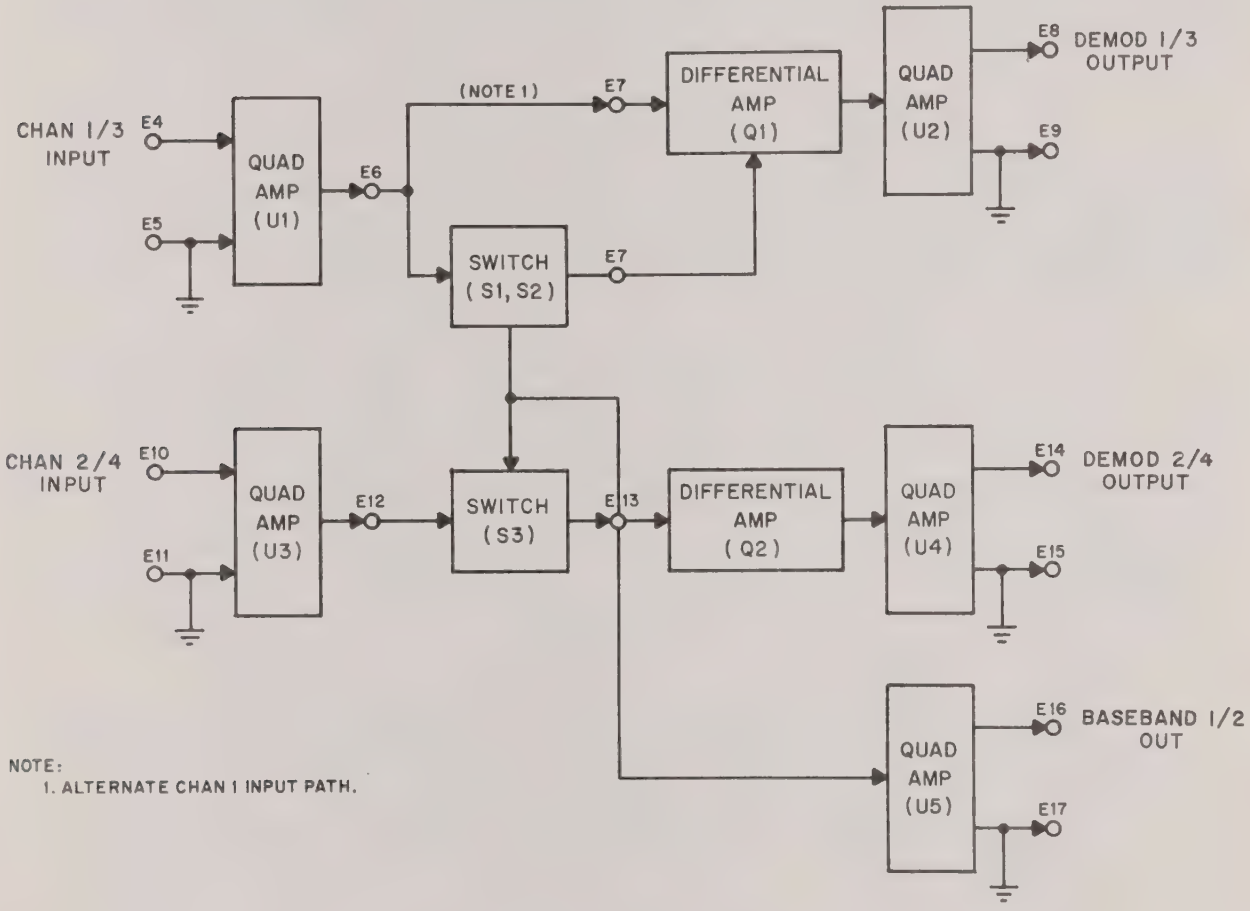


Figure 4-2. Baseband Signal Distribution Amplifier Block Diagram

Quad amplifier U2 is identical to U1 internally, but differs externally. Differential amplifier Q1 drives the input signal at E7 across resistor R13, which, in turn, is applied to U2C. The input signal is then applied to the bases of complementary emitter-followers U2B and U2D. This, along with feed-back through R16 and R17 to the emitter of Q1, furnish the gain required to obtain the proper signal level at E8. Resistor R19 establishes the source impedance at E8.

Quad amplifiers U3 and U4, differential amplifier Q2, and associated components perform the same functions for the CHAN 2 and CHAN 4 inputs as U1, U2, and Q1 perform for the CHAN 1 or CHAN 3 inputs described above.

Baseband output amplification is performed by quad amplifier U5 and associated components. U5 is a two-stage complementary amplifier with heavy feedback which results in

a very accurately tunable output impedance, low distortion, and good frequency response. Bias for U5 is divided in the same manner as for U3, except that diodes CR5 and CR6 are used in place of resistors. Each half of U5 performs in the same manner as the other half; therefore, only U5A and U5D are described in the following paragraph.

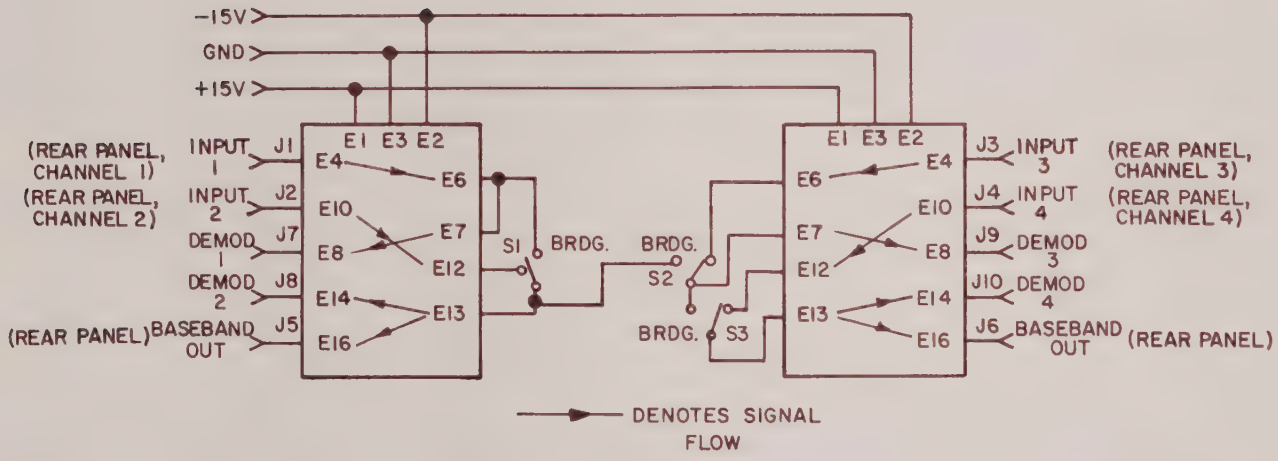


Figure 4-3. Baseband Signal Distribution Amplifier PC Assembly Block Diagram

Input signals from E13 applied to the base of U5A are developed across the collector of U5A and are, in turn, applied to the base of U5D. Resistor R53 provides emitter feedback and lowers distortion. The gain of the output stage is approximately 3 as determined by the ratio of R53 to R56. The heavy feedback from U5D is applied to the emitter of U5A through R59. Resistor R58 controls the amount of feedback. Adjustable resistor R58 allows setting the output amplitude to exactly that required by the system. Gain to the input amplifier-buffer, through a 93 Ω load, is set to unity.

4.3.3 DEMODULATOR POWER SUPPLY

The Demodulator power supply consists of power input circuitry, Power Supply Asembly A1A2, and power regulation circuitry as shown in Figure 4-4 and described in the following paragraphs. The power supply provides +15 Vdc, -15 Vdc, +5 Vdc, and an unregulated +8 Vdc to the Demodulator.

4.3.3.1 Power Input Circuitry

Refer to Figure 7-4 for the schematic diagram. In addition to the power supply cord and its associated connectors, the power input circuitry consists of filter FL1, power on/off switch S1 and its associated indicator DS1, fuses F1 and F2, voltage select switch S2, blower B1, and transformer T1.

With switch S1 in the ON position, either 115 Vac or 230 Vac is selected when switch S2 is applied to filter FL1. Filter FL1 decouples all inputs except the line voltage. It prevents input of external noise interference from the power source and also prevents feedback of random oscillations from the Demodulator back to the power source.

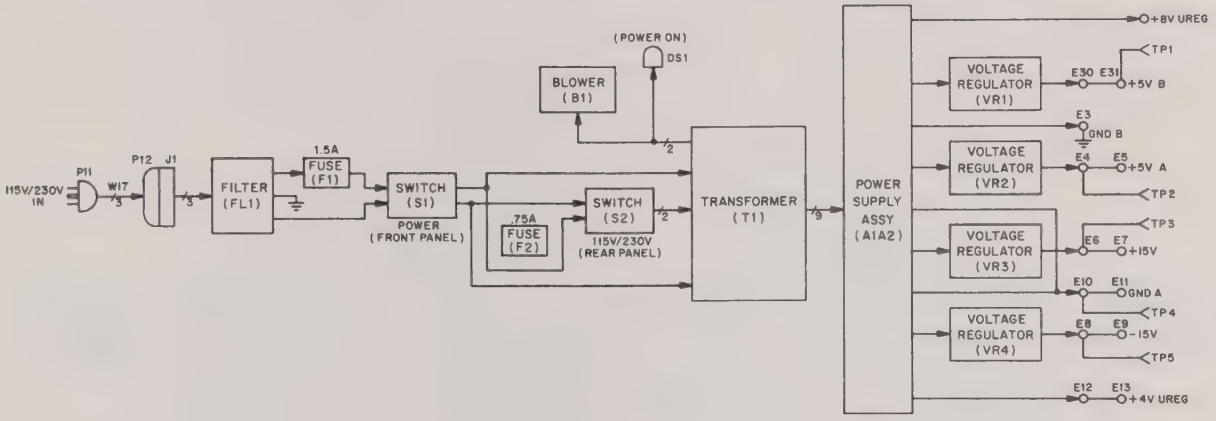


Figure 4-4. Demodulator Power Supply Block Diagram

Transformer T1 is a step-down transformer which has a dual primary with center-tapped secondaries. It provides a nominal 18.8 Vac, 7.3 Vac, and 34.5 Vac to power supply assembly A1A2 and 110 to 115 Vac to blower B1 and power-on indicator DS1. The separate 110 to 115 Vac to B1 and DS1 is at transformer terminals 14 and 15. The wiring from transformer T1 to power supply assembly A1A2 is isolated from the chassis to retain rectifier peak currents.

4.3.4 TYPE 766001 POWER SUPPLY ASSEMBLY (A1A2)

Refer to Figure 7-4 for the schematic diagram of Power Supply Assembly A1A2. The power supply assembly is comprised of four full wave rectifier circuits, CR1 and CR2, CR3 and CR4, and U1 along with their associated components.

Diodes CR1 and CR2 form the +9 volt unregulated supply for the demodulator power-up/power-down circuits and both +5 volt regulated supplies. A nominal 18.8 Vac is input from transformer T1 at input pins 4, 5, 6, and 7, 8, 9 to the anodes of CR1 and CR2, respectively. A center-tapped ground potential from T1 is available at input pins A, B, and C. The +9 volt unregulated output is at pins 1, 2, and 3.

Diodes CR3 and CR4 form the +4 volt unregulated supply for driving the displays in the demodulator units. A nominal 7.3 Vac is input from transformer T1 at input pins D, E and F, H to the anodes of CR3 and CR4, respectively. A center-tapped ground potential from T1 is available at input pins J and K. The +4 volt unregulated output is at pins 10 and 11.

Bridge rectifier U1 is a dual full-wave rectifier which provides the +20 volts and -20 volts for the +15 Vdc regulated supplies. A nominal 34.5 Vac is input from transformer T1 at input pins L, M and N, P to the two halves of the bridge circuit. A center-tapped ground potential from T1 is available at input pins R and S. The +20 volt unregulated output is at pins 12 and 13. The -20 volt unregulated output is at pins 14 and 15.

4.3.5 POWER REGULATION CIRCUITRY

Refer to Figure 7-4 for the schematic diagram. The power regulation circuitry consists of four voltage regulators VR1, VR2, VR3, and VR4 on the Demodulator rear panel. Voltage regulators VR1 and VR2 are 5 volt regulators; and voltage regulators VR3 and VR4 are +15 and -15 volt regulators, respectively.

The +9 volt unregulated output from power supply assembly A1A2 at pins 1, 2, and 3 is input to VR1 and VR2. Voltage regulator VR1 supplies regulated +5 Vdc for the control unit digital circuitry and voltage regulator VR2 supplies +5 Vdc for the demodulator unit digital circuits. The use of two voltage regulators prevents digital input signals to the Demodulator from interfering with the operation of individual demodulator units. The single point dc ground keeps signal coupling from the digital circuitry from interfering with signal coupling in the demodulator unit analog circuits. The +9 volt unregulated input is also used for sensing by the Demodulator power-up/power-down circuits.

The +20 and -20 volt unregulated outputs from power supply assembly A1A2 at pins 12 and 13, and pins 14 and 15 are input to VR3 and VR4, respectively. Voltage regulators VR3 and VR4 supply regulated +15 and -15 Vdc at a ±2% tolerance for use by the Demodulator.

The +4 volt unregulated output from power supply assembly A1A2 at pins 10 and 11 is used to drive the demodulator unit LED displays.

4.3.6 TYPE 796060 REFERENCE GENERATOR ASSEMBLY (A1A3)

The reference generator assembly, located behind the control unit and illustrated in Figure 1-3, consists of Reference Generator PC Assembly A1A3A1, the 1 MHz REF IN connector J1, and MCLK 1 through MCLK 4 output connectors J2 through J5, respectively. It converts an external 1 MHz input signal, applied to connector J1 on the rear panel, into a 2 MHz output for the four demodulator units. In the case of an absence of the external 1 MHz input, the contained logic circuitry switches to an independent 2 MHz source for use by the demodulator units.

4.3.6.1 Part 380084 Reference Generator PC Assembly (A1A3A1)

Refer to Figure 4-5 for the block diagram and Figure 7-6 for the schematic diagram of Reference Generator PC Assembly A1A3A1. A 1 MHz input to rear panel jack J1 is input to E3 via cable assembly W11. After being applied to line termination resistor R1, it is applied to the input of comparator U1.

Comparator U1 outputs two complementary pulses continuously at output pins 9 and 11. The two continuous pulses are differentiated into sharp spikes and applied to input pins 2 and 3 of NOR gate U5A. NOR gate U5A, by responding to either of the input pulses, performs as a frequency doubler and outputs a string of 2 MHz pulses at pin 1. These pulses, nominally 500 ns apart, are applied to input pins 1 and 9 of one shot U2A and U2B, respectively.

One shot U2A is set up by R10, C7, and C8, with a 250 ns time constant which results in a 2 MHz square-wave output at pin 13. Resettable one-shot U2B is set-up with a longer time constant with the result that, so long as there is an input signal at pin 9, there is no change in the output at pins 12 and 5. A lack of input at pin 9 causes a change in output at pins 12 and 5 which, in turn, is used to gate NOR gates U5B and U5D, respectively. NOR gates U5B, U5C, and U5D select either the output from one shot U2A or 2 MHz TCXO U3.

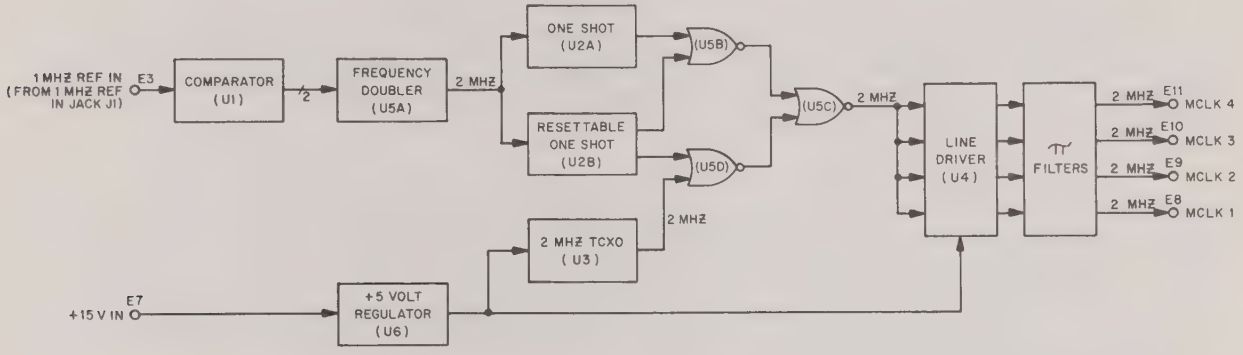


Figure 4-5. Reference Generator PC Assembly Block Diagram

The 2 MHz TCXO U3 supplies a 2 MHz output to input pin 12 of U5D. When gated by complementary U2B, gate U5D is enabled resulting in a 2 MHz input to pin 9 of U5C and gate U5B is disabled. U3 has its own separate power supply, +5 V regulator U6, which results in dual power regulation.

The selected 2 MHz output from U2A or U3 is applied in parallel to line driver U4. Line driver U4 has four filtered outputs, MCLK 1 through MCLK 4, which are used by the respective demodulator units as reference signals, described in paragraph 4.5.1.1.4.

4.4 CONTROL UNIT (A2)

The control unit provides the circuitry needed to implement the software program and thus control the Demodulator. Functional and circuit descriptions along with applicable block diagrams and schematics are provided for each major assembly of the control unit. The major assemblies are:

Type 796061 Motherboard (A2A1)
Type 796045 CPU Processor and Memory Bus Expansion Logic (A2A1A1)
Type 796046 Panel Interface and Demodulator Control (A2A1A2)
Type 796047-1 IEEE-488/RS-232 I/O Module (A2A1A3)

4.4.1 FUNCTIONAL DESCRIPTION

Refer to Figure 4-6 for the functional block diagram and Figure 7-7 for the schematic diagram of the control unit. The control unit consists of front panel mounted controls and indicators, three printed-circuit boards plugged into a motherboard, and interface connections. It provides the means of selection, tuning, and control of the four demodulator units in either a local or remote mode of operation. The selection, tuning, and control functions are performed by the control unit digital hardware and associated software routine.

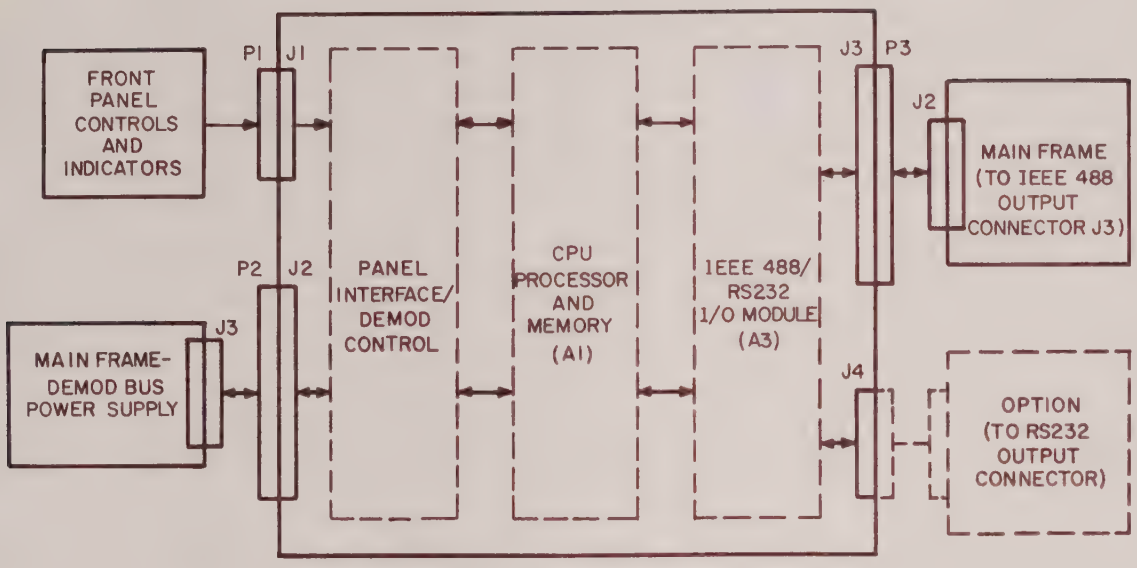


Figure 4-6. Control Unit Functional Block Diagram

Refer to Figure 4-7 for the functional block diagram for the control unit digital hardware. Microprocessor U1 reads information from memory, panel interface, demodulator interface, or IEEE-488 interface and then processes the information. It then writes information back to memory or the interfaces. The microprocessor communicates with and controls the digital circuits using a bi-directional data bus, address bus, and control bus.

Throughout the software routine, each of the four associated demodulator units and the control unit receives information from and sends information to the microprocessor. The IEEE-488 bus enables communication between the Demodulator and an outside controller using bit serial-byte parallel data format. The control unit front panel switches write information to the panel interface logic which is then input to the microprocessor. It, in turn, writes information to activate or change the appropriate demodulator unit.

4.4.2 TYPE 796061 MOTHERBOARD ASSEMBLY (A2A1)

Refer to Figure 7-8 for the schematic diagram of Motherboard Assembly A2A1. Motherboard A1 provides the mounting provisions and electrical interface for the three printed circuit boards used in the control unit. It also provides, via its own electrical connectors, electrical interfaces from the printed circuit boards to the control rack frame, and subsequently to the demodulator units and front and rear panel connectors, and to the control unit front panel controls and indicators.

4.4.2.1 Type 796045 CPU Processor and Memory Assembly (A2A1A1)

4.4.2.1.1 Functional Description

Refer to Figure 4-8 for the functional block diagram and Figure 7-9 for the schematic diagram of CPU Processor and Memory Assembly A2A1A1. The microprocessor-based computer used in the Demodulator is controlled by a pre-programmed instruction set.

The computer incorporates a memory that holds the program, peripherals that allow input/output communication, and a central processing unit that controls the activities of the other components.

The CPU Processor and Memory circuitry controls most of the activities of the Demodulator. The outputs include a clock frequency, 16 address lines, 10 control lines, and an 8-bit bi-directional data bus. The data bus is a bi-directional path on which data can flow between the processor and memory, the demodulator units, or the IEEE-488 bus. The address bus is a uni-directional group of lines that identify a particular memory location or I/O device. The control bus indicates the type of activity in progress.

The processor module, memory, and I/O circuitry are common to any computer system. It contains the CPU and system timing and interface circuitry. Timing control signals are provided by a 4 MHz crystal. The erasable/programmable read-only memory (EPROM) physically holds the program and the random access memory (RAM) is used for data storage and retrieval. Associated with the EPROM is a memory decode circuit that identifies what memory location the microprocessor is addressing. Power up/fail circuitry is provided to meet the unique power on requirements of the microprocessor. A backup battery provides voltage to retain RAM memories in case the demodulator is deenergized by either the operator or power failure.

The following is a brief functional description of each pin of the 8085A Microprocessor used in the demodulator. Refer to Figure 4-9 for the following description.

Pins X_1 and X_2 are connected to 4 MHz crystal Y1 to drive the internal clock generator. The 4 MHz input frequency is divided-by-two to establish the 2 MHz internal operating frequency. RESET OUT indicates CPU is being reset. The RESET OUT signal is synchronized to the processor clock and lasts an integral number of clock periods. SOD is the serial output data line which is reset by RESET IN signal. SID is the serial input data line. TRAP is a nonmaskable RESTART interrupt. RST 5.5, RST 6.5, and RST 7.5 are restart interrupts which cause an automatic insertion of an internal restart. INTR is an interrupt request which is used as a general purpose interrupt. AD_0 through AD_8 are multiplexed address/data bus. AD_0 through AD_7 represent the lower 8 bits of the memory address or I/O address which appear on the bus during the first clock cycle of a machine cycle and then becomes the data bus during the second and third clock cycles. V_{SS} supplies the ground reference. A_8 through A_{15} represent the most significant 8 bits of the memory address or I/O address. S_0, S_1, and IO/$\overline{M}$ are machine cycle status outputs. ALE is an address latch enablewhich occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. $\overline{WR}$ is the write control. A low level on $\overline{WR}$ indicates the data on the data bus is to be written into the selected memory or I/O location. $\overline{RD}$ is the read control. A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the data bus is available for the data transfer. A high READY during a read or write cycle indicates that the memory or peripheral is ready to send or receive data. A low READY indicates that the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. $\overline{RESET\ IN}$ sets the program counter to zero and resets the interrupt enable and HLDA flip-flops. CLK (OUT) is the clock output for use as a system clock. CLK (OUT) is 2 MHz. HLDA is hold acknowledge which indicates that the CPU has received the hold request and that it will relinquish the bus in the next clock cycle. HOLD indicates that another master is requesting the use of the address and data buses. V_{CC} supplies the +5 Vdc. For a more complete description of the 8085A Microprocessor, refer to the manufacturer's user's manual or component data sheet.

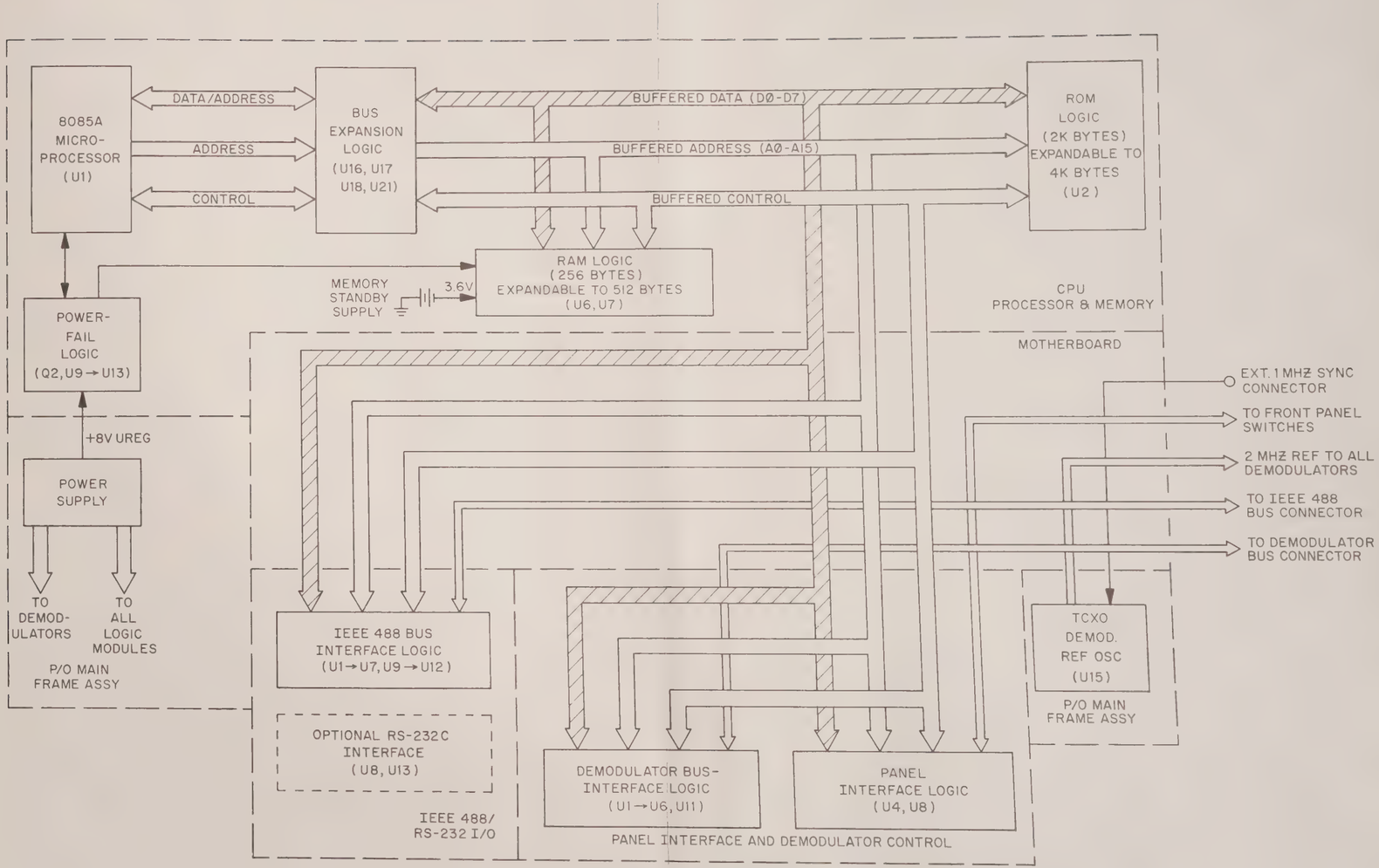

8085A MICRO-PROCESSOR (U1)
DATA/ADDRESS
ADDRESS
CONTROL
BUS EXPANSION LOGIC (U16, U17 U18, U21)
BUFFERED DATA (D0-D7)
BUFFERED ADDRESS (A0-A15)
BUFFERED CONTROL
ROM LOGIC (2K BYTES) EXPANDABLE TO 4K BYTES (U2)
MEMORY STANDBY SUPPLY
3.6V
RAM LOGIC (256 BYTES) EXPANDABLE TO 512 BYTES (U6, U7)
CPU PROCESSOR & MEMORY
MOTHERBOARD
POWER-FAIL LOGIC (Q2, U9→U13)
+8V UREG
POWER SUPPLY
TO DEMOD-ULATORS
TO ALL LOGIC MODULES
P/O MAIN FRAME ASSY
EXT. 1 MHZ SYNC CONNECTOR
TO FRONT PANEL SWITCHES
2 MHZ REF TO ALL DEMODULATORS
TO IEEE 488 BUS CONNECTOR
TO DEMODULATOR BUS CONNECTOR
IEEE 488 BUS INTERFACE LOGIC (U1→U7, U9→U12)
OPTIONAL RS-232C INTERFACE (U8, U13)
IEEE 488/ RS-232 I/O
DEMODULATOR BUS-INTERFACE LOGIC (U1→U6, U11)
PANEL INTERFACE LOGIC (U4, U8)
PANEL INTERFACE AND DEMODULATOR CONTROL
TCXO DEMOD. REF OSC (U15)
P/O MAIN FRAME ASSY

Figure 4-7. Control Unit Digital Hardware Block Diagram

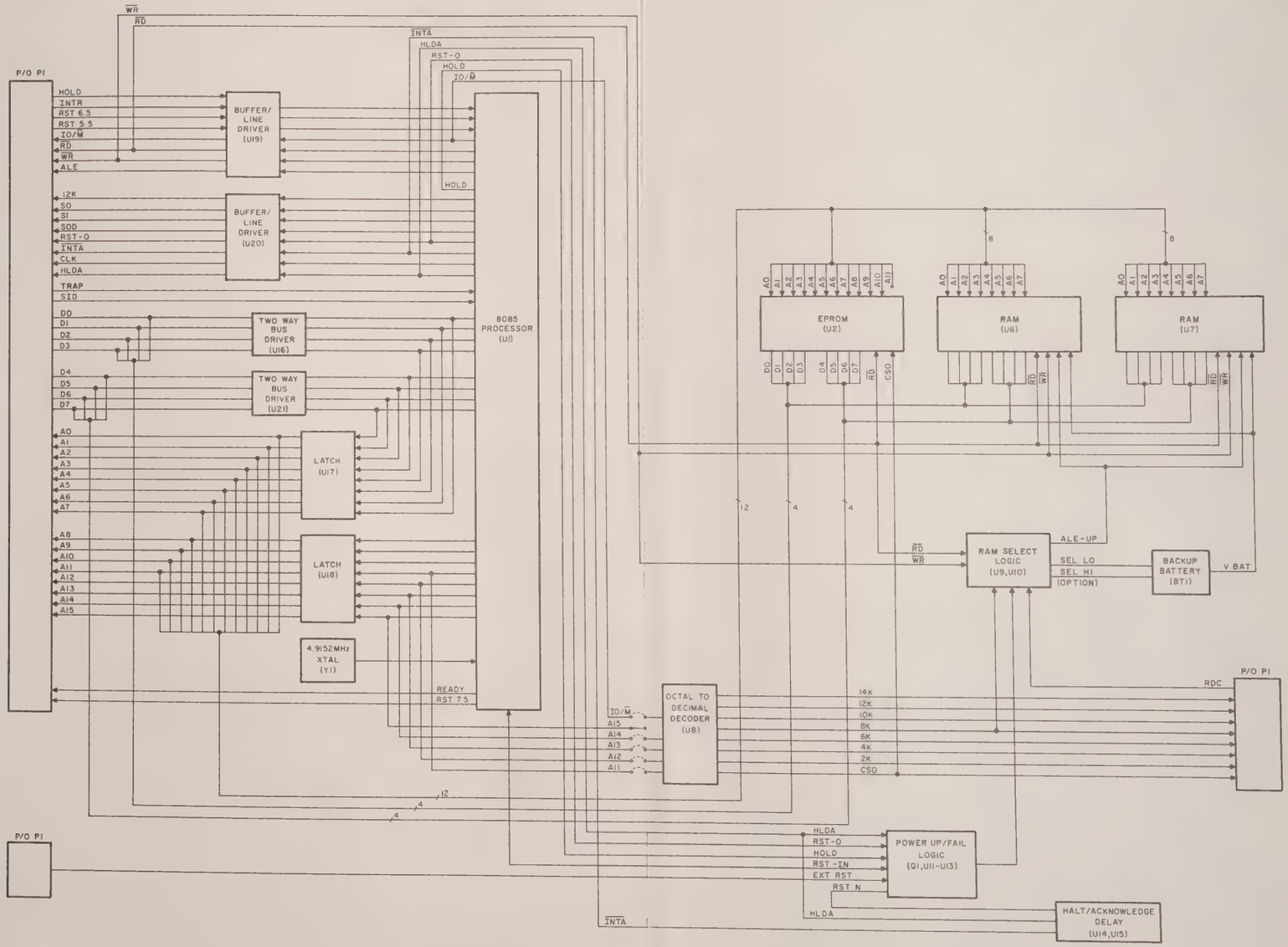
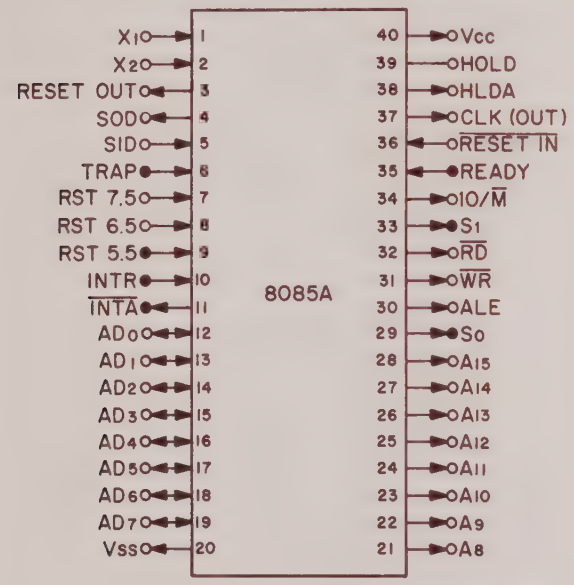


Figure 4-8. CPU Processor and Memory Functional Block Diagram

4.4.2.1.2 Circuit Description

Microprocessor U1 is a complete 8-bit parallel, central processing unit. It interfaces with the memory address lines and the data bus through bus drivers U16 and U21 and latches U17 and U18. Crystal Y1 generates a 4 MHz signal which is divided by two by the processor's internal clock generator to establish a 2 MHz internal clock frequency.

U2 is a 2,048-byte erasable/programmable, read only memory (EPROM). It has a non-volatile memory; the memory is retained when power is removed. The pre-programmed instruction set which controls the microprocessor, and, in turn, the demodulator is stored in U2. When an up to 11-bit address (A0 through A10) is input to U2 and the chip enable (CE) input is low, the addressed data is supplied on the eight output lines (00 07) 120 ns after the falling edge of a read ($\overline{RD}$) input at the output enable (OE) input.



NOTES:
1. ARROWHEADS INDICATE INPUT/OUT WITH ARROWHEADS POINTING TOWARD BODY BEING INPUTS.
2. ● DENOTES PINS NOT USED IN THIS APPLICATION.

Figure 4-9. Microprocessor Pin Assignments

U6 and U7 are 256 X 4-byte random access memories (RAMs). They are temporary storage elements that can be either written into or read by the microprocessor. Being temporary storage elements, U6 and U7 cannot retain memory with demodulator power removed without the use of backup battery BT1 and the power up/fail logic described in the following paragraphs. Memory address location and selection is performed by octal-to-decimal decoder U8 and RAM select logic U9 and U10. During a read cycle, the falling edge of the input at CE latches the input address word into on-chip registers. After the required address setup and hold times, the lines may be read when inputs CE, CS1, and CS2 are all low and input R/$\overline{W}$ is high. During a write cycle, the falling edge of the input at CE latches the addresses into on-chip registers. After the required data setup and hold times, the lines may be read when inputs CE, CS1, CS2 and R/$\overline{W}$ are all low simultaneously. The write portion of the cycle is terminated by the first rising edge on inputs CE, CS1, CS2, or R/$\overline{W}$.

The microprocessor utilizes 2,256 address locations, Figure 4-10, of 64,000 available address locations. The first 2,000 address locations (from 0 to 2,048) are used as CPU EPROM and 256 address locations (from 8,192 to 8,348) are used as CPU RAM. The microprocessor utilizes 128 I/O address locations of 256 available I/O address locations. These locations (from 0 to 127) have the same numerical values as the first 128 address locations used as CPU EPROM but are distinguished by means of the IO/$\overline{M}$ output from microprocessor pin 34.

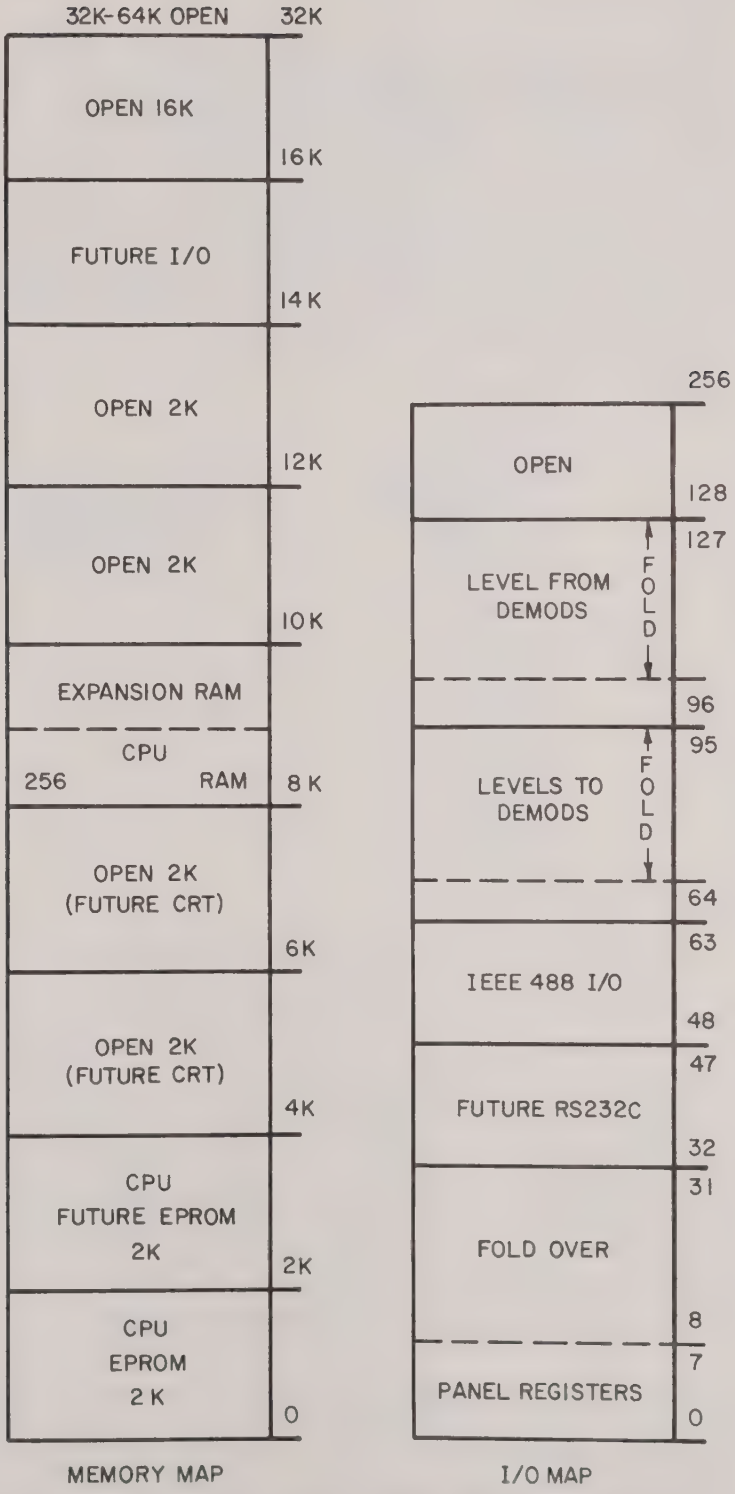


Figure 4-10. Processor Memory and I/O Maps

Octal-to-digital decoder U8 provides the address decode circuitry for EPROM U2 and in conjunction with RAM select logic U9 and U10, provide the address decode circuitry for RAMs U6 and U7. For example, EPROM U2's location per the memory map is address locations 0 to 2,000 (decimal). The falling edge of an output at output Y0 of U8, which is the 0 to 2k line, is applied to the CE input of EPROM U2, enabling it as the addressed location. RAMs U6 and U7 have an address of 8k. The falling edge of an output at output Y4 of U8, which is the 8k line, is applied to RAM Select Logic U10 and U9 where, along with the low output from single shot U13, (part of the power up/fail logic) and the low input on line A8, provide low inputs to inputs CS1 and CS2 on U6 and U7. The falling edge of an input on ALE provides the third low at RAM input CE, all three of which are necessary to read from or write to RAMs U6 and U7.

Backup battery BT1 retains RAM memory for up to approximately 700 hours when the Demodulator is deenergized. It is kept fully charged, when the Demodulator is energized, via diode CR3 and resistor R5. When the Demodulator is deenergized, the +5 V regulated supply voltage drops to zero and CR3 becomes reversed-biased, preventing BT1 from discharging through Demodulator circuitry.

Power Up/Fail Logic Q1, U11, U12, and U13 protect the RAM memories during both long and short duration power interruptions. With an unregulated +10 to +12 V input at RDC, the output from single shot U13 is low. If the input at RDC drops below an unregulated +8 V, the output from U13 goes high which is applied to U10. A high input to U10 causes a high output from U9 which is applied to inputs CS1 and CS2 on U6 and U7.

4.4.2.2 Type 796046 Panel Interface and Demodulator Control Assembly (A2A1A2)

4.4.2.2.1 Functional Description

Refer to Figure 4-11 for the functional block diagram and Figure 7-10 for the schematic diagram of Panel Interface and Demodulator Control Assembly A2A1A2. The panel interface and demodulator control modifies and interfaces control unit front panel switch data with the computer, described in paragraph 4.4.2.1, and provides interfaces between the computer and the demodulator units via the demodulator bus.

4.4.2.2.2 Circuit Description

Control unit front panel switch status changes are input to debounce modules U7, U8, and U9. The debounce modules, also known as digital contact bounce eliminator circuits, take input signals from bouncing contacts, stabilize them and then generate clean digital signals four clock periods after the inputs have stabilized. Dual 4-bit divider U14 provides an adjustable slower clock for U7, U8, and U9. The digital signal outputs are then passed through I/O U4 Ports A and B, as applicable, to connector P1, where they are output to CPU processor and memory.

Detected AGC from an active demodulator unit is sent from its respective AGC IF amplifier Q4 (Figure 7-19) via average detector CR2 and buffer U2A on IF demodulator A1A6 through the demodulator bus to connector P1. This AGC analog level is available at pins 40, 42, 41, and 44 of connector P1 for demodulator units one through four, respectively.

The AGC analog level is passed through analog switch U11 by a low (0 volt level) at A1 through A4. Assuming a low input at A1 and highs at A2 through A4, the AGC analog data for demodulator unit one is passed through U11 to quad operational amplifiers U5 and U6 where it compared against voltage levels established by the precision resistor divider R1 through R8 to establish the switching points for U5 and U6. The following comparator input voltages establish the switching points for the demodulator unit Audio Output Level.

(This page intentionally left blank.)

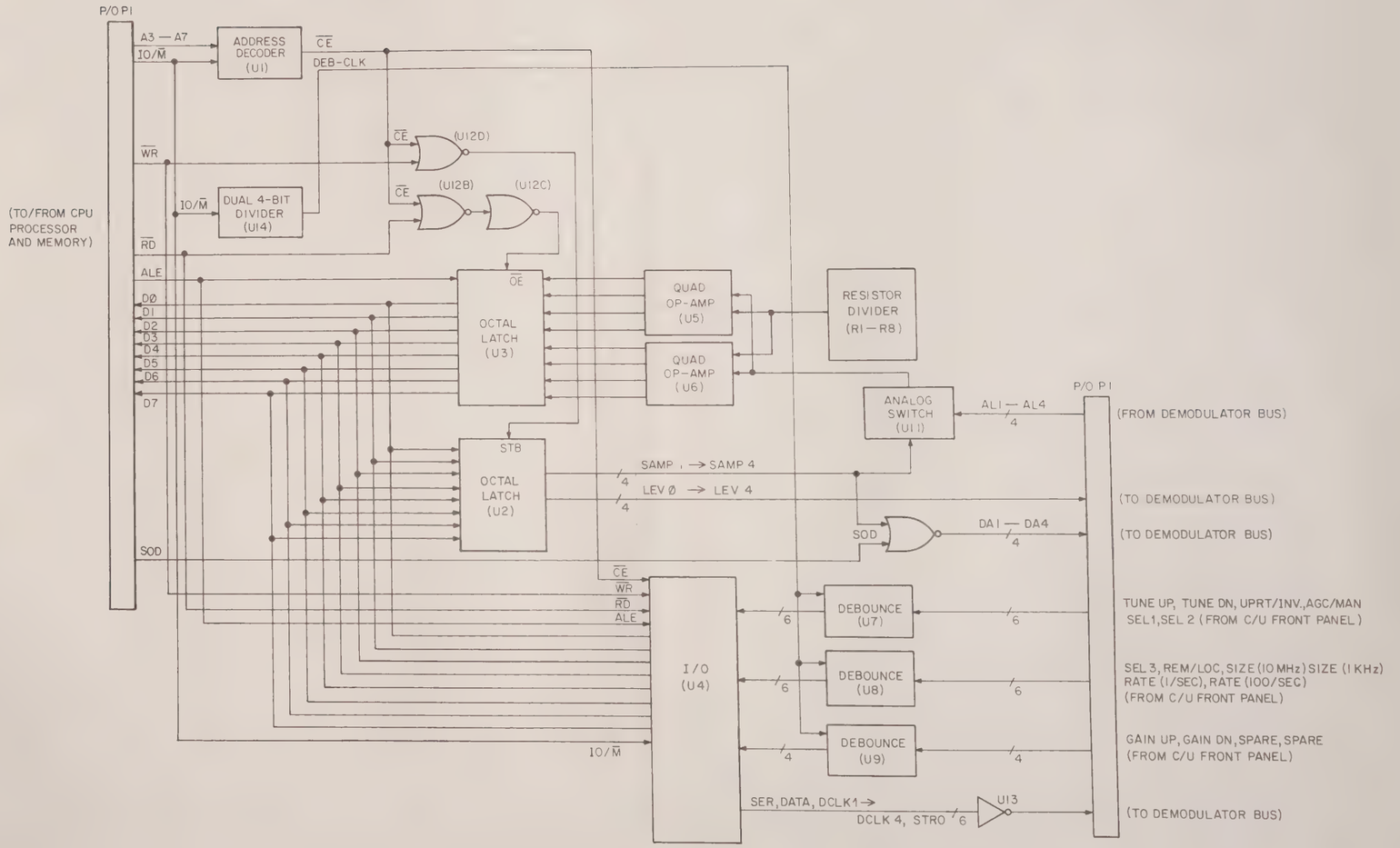


Figure 4-11. Panel Interface and Demodulator Control Functional Block Diagram

Audio Output Level	Comparator Input Voltage
Over	2.95
-2	2.65
-3	2.36
-4	2.11
-5	1.89
-6	1.68
-7	1.50
-8	1.35
Under	(None)

The comparator outputs are latched at octal latch U3 until enabled by ALE (pin 11) and $\overline{RD}$ (pin 9). The outputs from U3 are then fed onto the microprocessor data bus and sent to the microprocessor via pins 51, 58, 52, 50, 61, 66, 59, and 55 of connector P1, where the eight high/low states are converted into one 4-bit word. Depending upon the AGC level analog and active demodulator unit, a 4-bit word defining the AGC analog level (LEV 0 through LEV 3) is returned to octal latches U2.

Selection of a demodulator unit is performed at Gate U10 when a SOD LOW is combined with a low resulting in an out to D-type flip-flop U3 on motherboard assembly A3A1, described in paragraph 4.5.2. This +5 V level is applied to the U3 clock input (pin 9) which unlatches U3, passing the 4-bit word containing the AGC data through the display driver, described in paragraph 4.5.3, to BCD-to-decimal decoder/driver U1 on the display board, described in paragraph 4.5.3.3.2.

4.4.2.3 Type 796047-1 IEEE-488/RS-232 I/O Assembly (A2A1A3)

4.4.2.3.1 Functional Description

Refer to Figure 4-12 for the functional block diagram and Figure 7-11 for the schematic diagram of IEEE-488/RS-232 I/O Assembly A2A1A3. The IEEE-488/RS-232 I/O, along with IEEE STD 488 PORT on the rear panel of the control rack frame, provide the interface between the demodulator and the IEEE-488 Bus. It contains an MC68488 general purpose interface adapter (GPIA) and the necessary external logic to establish data flow to and from the CPU processor and memory and external instruments/controllers.

GPIA U7 connects to the microprocessor via an 8-bit bi-directional data bus (D0 through D7) and various control lines and external logic which enable selection and control of U7 and, in turn, the IEEE-488 Bus. These control lines include a chip select ($\overline{CS}$), a read/write (R/$\overline{W}$), and reset ($\overline{RST}$), three register selects (RS0, RS1, RS2), an interrupt-request ($\overline{IRQ}$), and an address switch enable (ASE). The external logic includes address decoder U1 and bus select logic U5 and U6 which enable the microprocessor to address U7, and instrument address switch S3 and buffer U3 which enable setting the address of an external controller or instrument.

GPIA U7 connects to the IEEE-488 output through four line drivers, or bus transceivers, which buffer the 488 data bus. The line drivers are controlled by transmit/receive control signals T/$\overline{R}$1 and T/$\overline{R}$2 from U7. Line drivers U9 and U10 are used to control the 8-bit bi-directional data bus (D101 through D108) and line drivers U11 and U12 are associated with Bus Handshake and Bus Management.

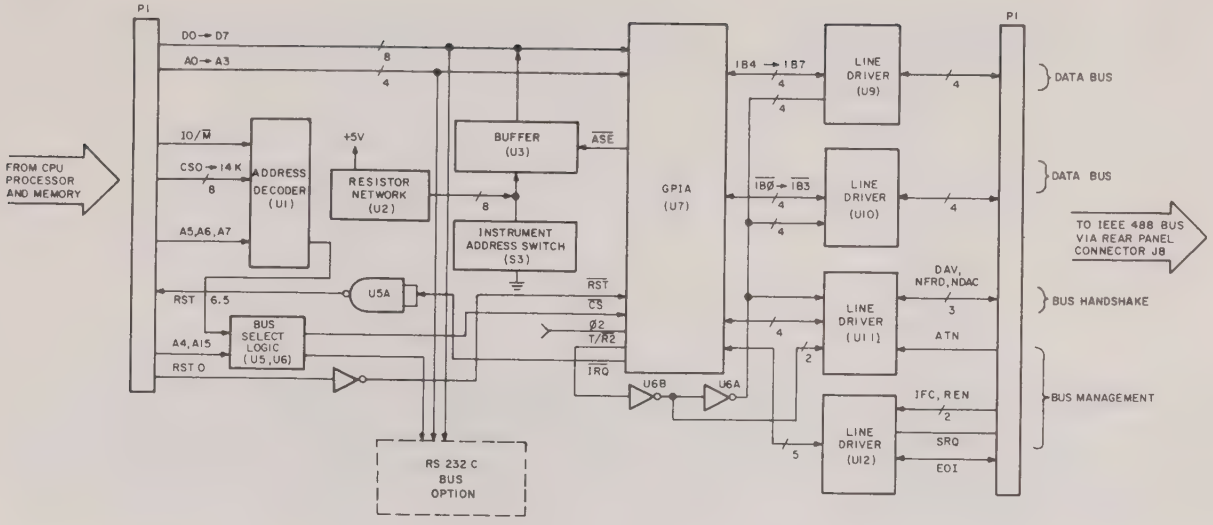


Figure 4-12. IEEE-488/RS-232 I/O Functional Block Diagram

Prior to any byte transfer from a talker to one or more listeners, a handshaking procedure, Figure 4-13, is performed. The handshake procedure ensures that each listener is ready to accept data; the data on the data bus is valid; and the data has been accepted by all acceptors.

With both the talker and listener in power-up or start in a known quiescent state, the source has data valid (DAV) high, indicating the data on the bus is not valid. The listener sets both not ready for data (NRFD) and not data accept (NDAC) passive true (low), which indicates that the listener is not ready to accept data and that no data has been accepted. When ready to accept data, a listener sets NRFD high. When all listeners have set NRFD high, then the talker can assert DAV indicating data is valid. If both NRFD and NDAC are sensed high by the source, an error condition exists.

The acceptors respond by pulling NRFD low enabling data transfer. Data is now transferred at a speed which can be handled by the slowest listener on the bus. As each listener accepts the transferred data, it sets its NDAC handshake line high. The talker does not see NDAC high until the slowest listener responds. When the slowest listener responds, NDAC goes high. The NDAC high is sensed by the talker and sets DAV high, indicating that the data on the data bus is no longer valid. When DAV goes high, the listener returns the NDAC line low. This cycle repeats itself for each data byte.

Five Bus Management lines maintain an orderly flow of data across the interface lines. They are attention (ATN), interface clear (IFC), remote enable (REN), service request (SRQ), and end or identify (EOI) with ATN being associated with line driver U11 and the rest, line driver U12.

ATN is set low by the controller to disable current talkers and listeners, freeing the data bus. During the low, devices monitor the data bus for addressing or an interface command. Data flows on the data bus when ATN is inactive (high). IFC, when brought low, puts GPIA U7 into a known quiescent state to provide a known reference for system operations.

SRQ, when low, indicates to the controller that a device on the bus is in need of service. It also is used to request an interruption in the current sequence of events. EOI is used to signal the end of a multiple byte transfer and in conjunction with ATN executes a parallel polling sequence.

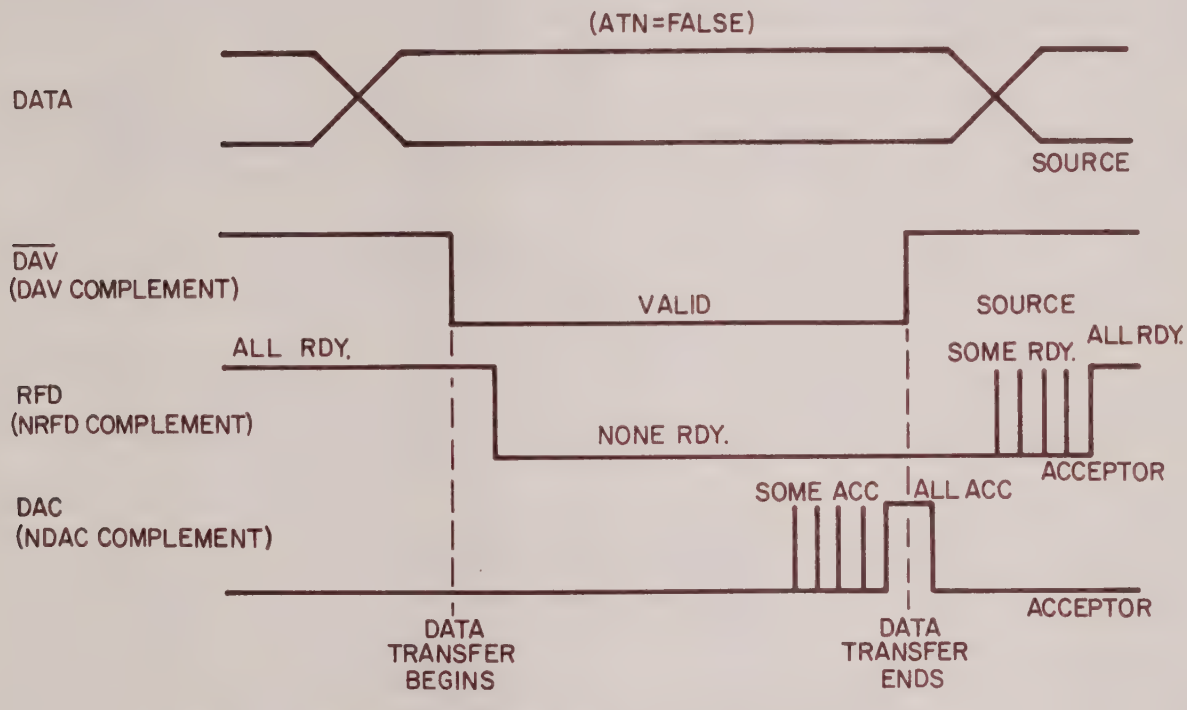


Figure 4-13. Demodulator to IEEE-488 Bus Handshake Timing

4.4.2.3.2 Circuit Description

For the purposes of this description, assume that the following address is input to connector P1.

A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	1	0	1	1

The IEEE bus, map location 48, is selected as follows. Address lines A5, A6, and A7 to select inputs A, B, and C of address decoder U1 are high, low, and low representing 32. Enable inputs G2B, G2A, and G1 are low, low, and high, respectively. This results in data

output Y1 being low, representing 32. This low is inverted by U6. Address line A4, representing 16, is high. The high output of U6, representing 32, and the high on address line A4, representing 16, are input to U5 with a resulting low output, representing 48. This low is applied to chip select ($\overline{CS}$) input of GPIA U7.

Address lines A2, A1, and A0 are register select lines (RS0 through RS2 on U7) for the seven write-only and eight read-only registers. Address line A3 is the read/write (R/$\overline{W}$) line for the registers. With inputs on A3, A2, A1, and A0 being high, low, high, and high, respectively, read-only register three will be read.

Resistor network U2 provides a 5-volt pullup for instrument address switch S3. Switch S3 sets the address of the Demodulator on power-up. A low output on the address switch enable ($\overline{ASE}$) line from U7 enables tri-state buffer U3, which allows the address set in S3 to be read on data lines D0 through D7.

Line drivers U9 through U12 are bi-directional bus transceivers which provide the interfaces between the TTL logic of the Demodulator and the IEEE-488 instrumentation bus.

Line drivers U9 and U10, associated with the data bus, enables transmission from U7 to the IEEE-488 Bus upon receipt of a high transmit/receive control signal (T/$\overline{R}$2) from U7; Demodulator as talker. Conversely, upon receipt of a low input (T/$\overline{R}$2), data is transmitted from the IEEE-488 Bus to U7 and, in turn, to the microprocessor; Demodulator as listener.

Line driver U11, associated with the demodulator to IEEE-488 Bus handshake, enables transmission/receipt of the data valid (DAV), ready for data (RFD), and data accepted (DAC) bits. The data valid line is enabled for transmission from U7 to the IEEE-488 Bus upon receipt of a high T/$\overline{R}$2 input and enabled for receipt by a low T/$\overline{R}$2 input. The ready for data (RFD) and data accepted (DAC) are enabled for transmission by a low T/$\overline{R}$2 and for receipt by a high T/$\overline{R}$2. For further information regarding the handshake, refer to the description in paragraph 4.4.2.3.1 or the appropriate manufacturer's user's handbook or component data sheet. The attention (ATN) bit, associated with the bus management, is input to U7 from the controller via U11 as a low to free signal lines $\overline{IB0}$ through $\overline{IB7}$.

Line driver U12, associated with bus management, enables receipt of interface clear (IFC) and remote enable (REN), transmission of service request (SRQ), and transmission/receipt of end or identify (EOI).

4.5 DEMODULATOR UNITS A3, A4, A5, A6

As stated in paragraph 4.1, since all four demodulator units are identical to each other, the theory of operation of only one, assembly A3, is described in the following paragraphs. Refer to Figure 4-14 for the functional block diagram of a demodulator unit.

4.5.1 FUNCTIONAL DESCRIPTION

Baseband signal inputs, from 200 Hz to 308 kHz, from the baseband signal distribution amplifier on the control rack frame, described in paragraph 4.3.2, are processed by Input Converter Assembly A1A4 to produce a 2.0 MHz IF output and an analog output.

The 2.0 MHz IF output from the input converter is fed to 2 MHz Filter FL1. Filter FL1 is a delayed equalized filter which passes the desired sideband while suppressing an unwanted sideband by 45 dB. The filtered output from FL1 is fed to IF Demodulator Assembly A1A6 which mixes the filtered output from FL1 with the 2 MHz input from the reference

buffer. The resultant audio signal is fed to the demultiplexed output on the rear panel of the control rack frame and to Attenuator Control Assembly A1A5. When enabled by an audio switch, the audio input from the IF demodulator is passed through the attenuator control to the phones jack on the front panel of the control unit.

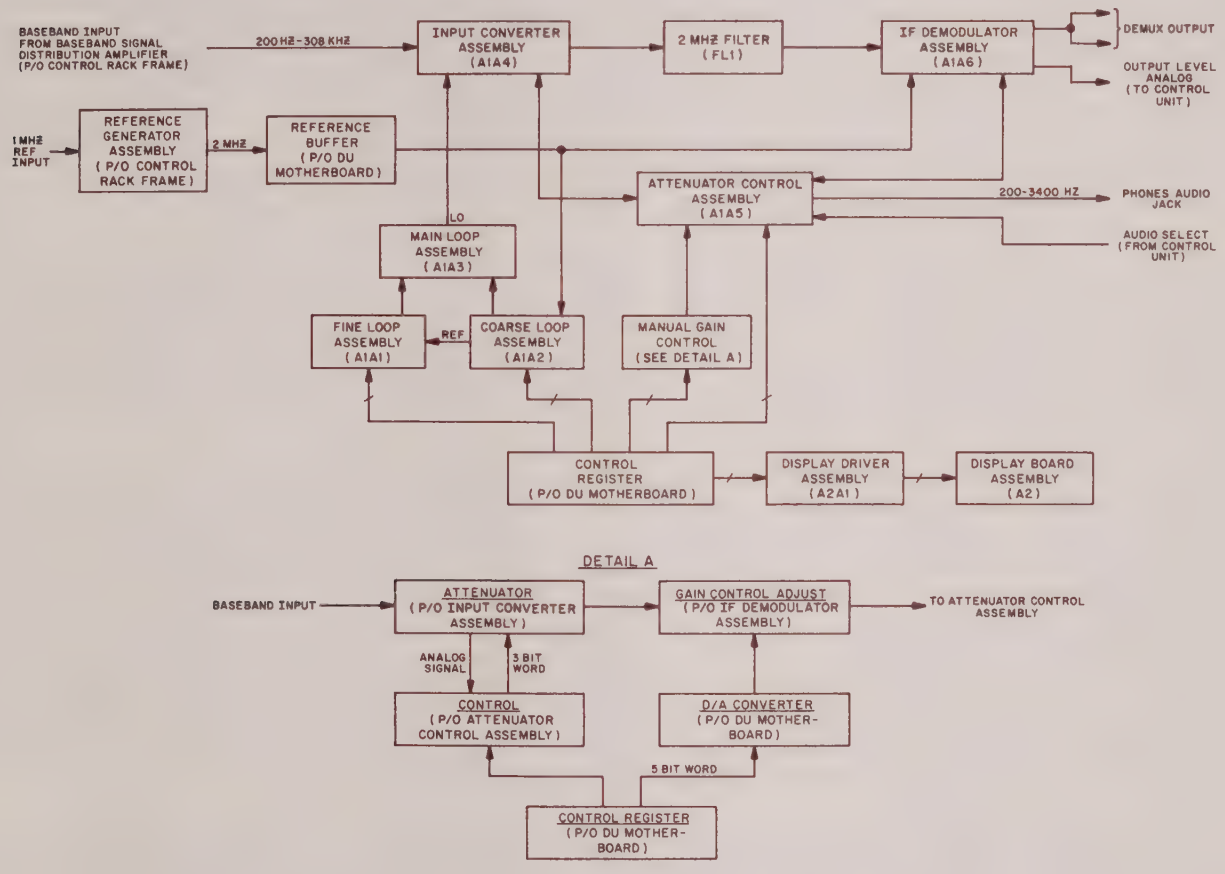

BASEBAND INPUT FROM BASEBAND SIGNAL DISTRIBUTION AMPLIFIER (P/O CONTROL RACK FRAME)
200 HZ-308 KHZ
INPUT CONVERTER ASSEMBLY (A1A4)
2 MHZ FILTER (FL1)
IF DEMODULATOR ASSEMBLY (A1A6)
DEMUX OUTPUT
OUTPUT LEVEL ANALOG (TO CONTROL UNIT)
1 MHZ REF INPUT
REFERENCE GENERATOR ASSEMBLY (P/O CONTROL RACK FRAME)
2 MHZ
REFERENCE BUFFER (P/O DU MOTHERBOARD)
ATTENUATOR CONTROL ASSEMBLY (A1A5)
200-3400 HZ
PHONES AUDIO JACK
AUDIO SELECT (FROM CONTROL UNIT)
LO
MAIN LOOP ASSEMBLY (A1A3)
FINE LOOP ASSEMBLY (A1A1)
REF
COARSE LOOP ASSEMBLY (A1A2)
MANUAL GAIN CONTROL (SEE DETAIL A)
CONTROL REGISTER (P/O DU MOTHERBOARD)
DISPLAY DRIVER ASSEMBLY (A2A1)
DISPLAY BOARD ASSEMBLY (A2)
DETAIL A
BASEBAND INPUT
ATTENUATOR (P/O INPUT CONVERTER ASSEMBLY)
GAIN CONTROL ADJUST (P/O IF DEMODULATOR ASSEMBLY)
TO ATTENUATOR CONTROL ASSEMBLY
ANALOG SIGNAL
3 BIT WORD
CONTROL (P/O ATTENUATOR CONTROL ASSEMBLY)
D/A CONVERTER (P/O DU MOTHER-BOARD)
5 BIT WORD
CONTROL REGISTER (P/O DU MOTHER-BOARD)

Figure 4-14. Demodulator Unit Functional Block Diagram

The analog output from the input converter is fed to Attenuator Control Assembly A1A5 which compares the analog signal with an established reference and converts the difference into digital form. The digital word is then output back to the input converter assembly to select attenuation to be placed on the baseband signal input path.

The 2 MHz signal from the reference generator assembly, described in paragraph 4.3.6, is input to the reference buffer on the demodulator unit motherboard. The reference buffer, in turn, feeds the 2 MHz signal to the IF demodulator and Coarse Loop Assembly A1A2. The 2 MHz input to the IF demodulator is mixed with the filtered signal input from filter FL1. The 2 MHz input to the coarse loop is divided for use as part of the synthesizer operation described in paragraph 4.5.2.

Refer to Detail A of Figure 4-14 for the following description. The manual gain control, on the demodulator unit motherboard, is a digital-to-analog converter which converts a

5-bit word containing manual gain data from the control register into an analog signal which is output to the IF demodulator where a gain control adjust circuit provides the AGC output to the attenuator control.

The control register, located on the demodulator unit motherboard, is divided into two parts. The first part is a 4-bit latch register which receives output level control data from the control unit. The output level control data is multiplexed in the control unit from an analog voltage provided by the attenuator control via the IF demodulator. The encoded output level control data is then returned to the demodulator unit for decoding by a BCD-to-decimal decoder on Display Board Assembly A2. The second part is a group of 8-bit shift registers with a parallel latch. Five registers, located on the demodulator unit motherboard, receive data from the control unit for use by the synthesizer and two registers, located on Display Driver Assembly A2A1, are used with the front panel display.

The front panel display, located on Display Board Assembly A2, consists of five digits of a seven-segment display, a bar display with ten LEDs, and various other LED indicators as INVERT/ERECT and LCL/RMT. After decoding by a BCD-to-decimal decoder, on the display board, the gain data from the control unit is displayed on the bar display. Serial data from the control unit, decoded by the registers discussed in the previous paragraph, is displayed on the balance of the indicators.

The synthesizer consists of Main Loop Assembly A1A3, Coarse Loop Assembly A1A2, and Fine Loop Assembly A1A1 (Figure 4-15) all of which work in conjunction with each other to produce a controllable LO output signal to the input converter. The fine loop provides the capability of increasing or decreasing the LO signal step size in 10 Hz steps while the coarse loop provides the capability of increasing or decreasing the step size in 10 kHz steps. The 2 MHz reference signal input to the coarse loop is divided and applied to a programmable phase lock loop and to another divider. The phase lock loop contains a phase frequency detector, an active integrating filter, a voltage-controlled oscillator, and a programmable divider all of which provide a frequency output which may be increased or decreased. The output from this circuit is applied to a double-balanced mixer in the main loop. The reference input signal is also divided-by-10 and applied to the fine loop.

The fine loop contains a phase lock loop and a divide-by-100 divider. The fine loop phase lock loop, functionally, is the same as that for the coarse loop, except that its frequency output may be increased or decreased in 10 Hz steps. The output from this circuit is applied to a divide-by-100 divider and applied to the phase frequency detector in the main loop.

The main loop contains a phase lock loop with a double-balanced mixer in its feed-back circuit and an output divider. The input to the double-balanced mixer from the coarse loop, which after being mixed with the voltage-controlled oscillator output, is applied to the phase detector along with the output from the fine loop. As a result, the main loop phase lock loop output is increased or decreased, dependent upon changes to the coarse loop and/or the fine loop. The phase lock loop output is divided and applied to the input converter.

4.5.2 TYPE 796070 MOTHERBOARD ASSEMBLY (A1)

Refer to Figure 4-16 for the functional block diagram and Figure 7-13 for the schematic diagram of Motherboard Assembly A1. The demodulator unit motherboard, in addition to providing electrical interfaces for six of the eight PC assemblies associated with the demodulator unit, contains five of the seven shift registers of the control register, a 2 MHz buffer and analog amplifier, and a digital-to-analog converter.

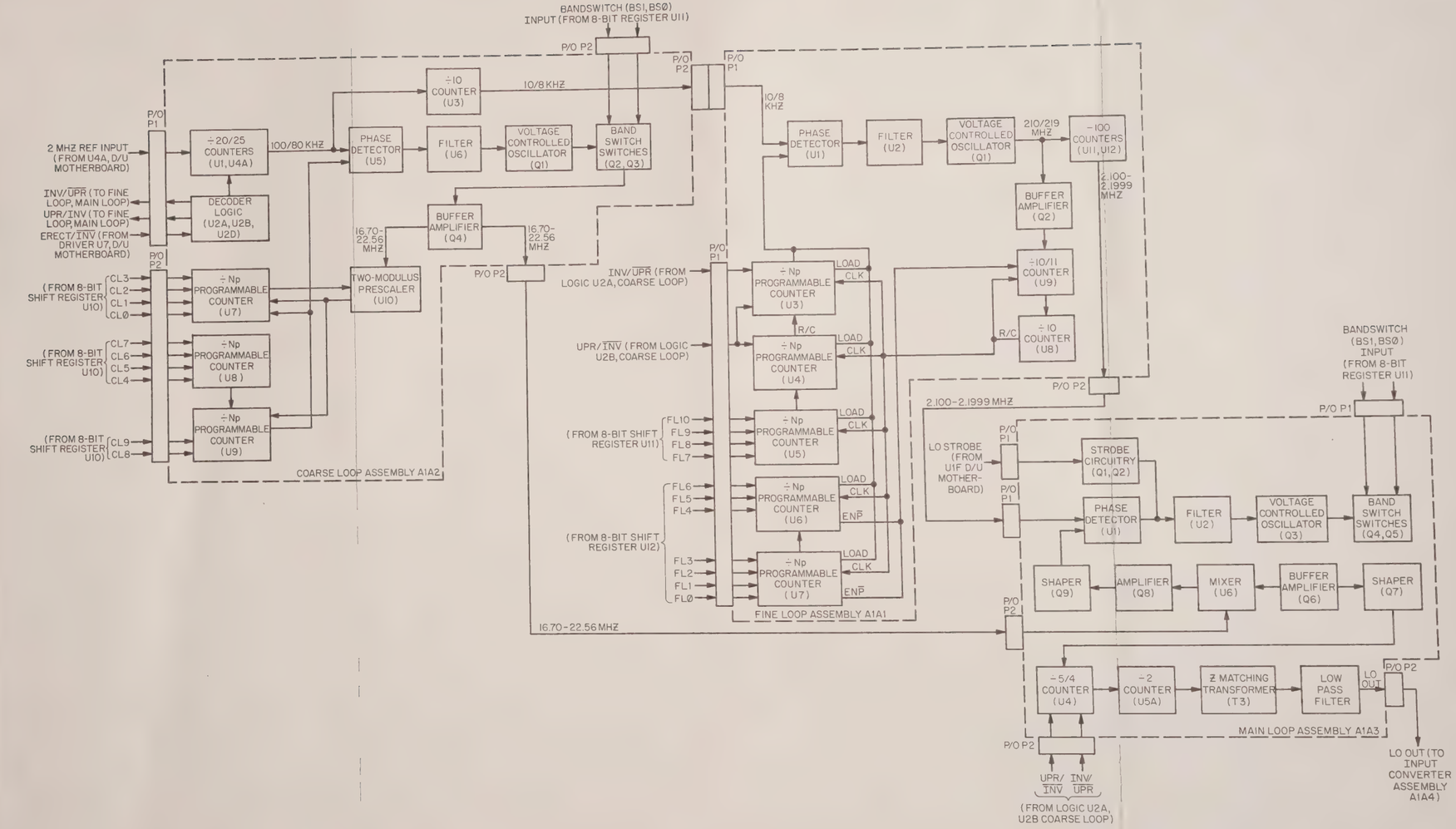


Figure 4-15. LO Synthesizer Functional Block Diagram

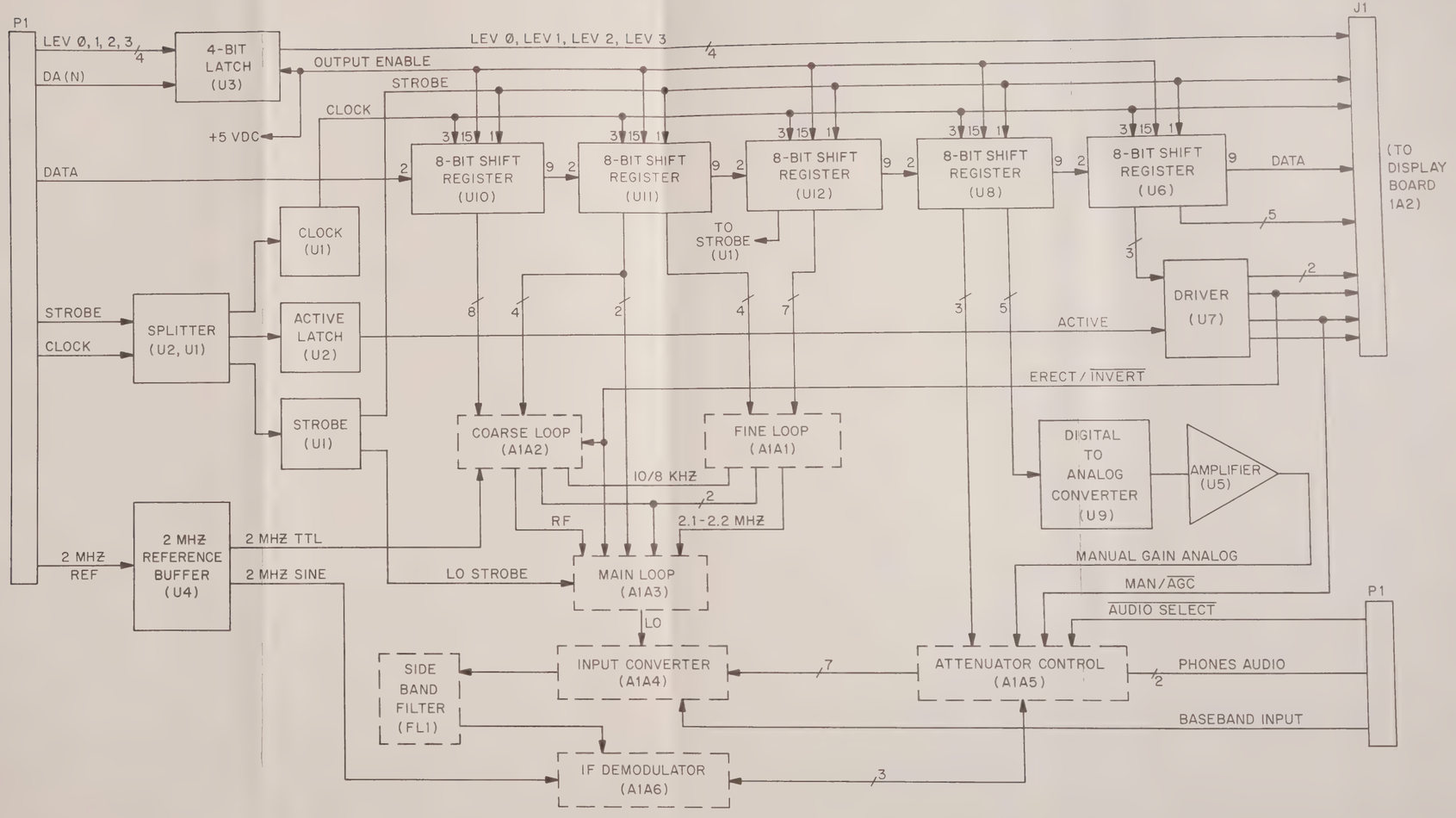


Figure 4-16. Demodulator Unit Motherboard Assembly Block Diagram

4.5.2.1 4-bit Latch U3

LEV 0, 1, 2, and 3 data, which originate in the control unit, are input to 4-bit latch U3 on input pins 12, 4, 13, and 5. With clear input pin 1 tied high to +5 Vdc, data at the input pins are transferred to output pins 10, 2, 15, and 7 during receipt of the positive-going edge of the DA(N) pulse at input pin 9. The output data from U3 are passed through Display Driver via Assembly A2 connectors J1 and J6 to input pins 15, 14, 13, and 12 of BCD-to-decimal decoder/driver U1 on the Display Board Assembly A2A1 where the data are decoded to drive the dBm OVER/UNDER indicators.

4.5.2.2 8-Bit Shift/Storage Registers U10, U11, U12, U8, and U6

Shift/storage registers U10, U11, U12, U8, and U6, along with shift/storage registers U1 and U2 on the display driver, and their associated logic circuits form the demodulator unit control register. They control the demodulator unit assemblies by decoding and routing the serial data input from the control unit.

Serial data, Figure 4-17, which originates in the control unit, are input to shift/storage register U10 at input pin 2. Data in the shift register is output, via pin 9, to the input pin, pin 2, of the next register on the positive-going edge of a clock pulse at input pin 3. The data is shifted bit-by-bit from register U10 down the string to register U6 until the control register is full or until the proper data registration occurs at the associated parallel latch. A positive-going strobe pulse from the control unit, at pin 7 of connector P1 passes through logic circuitry U1 and is applied in parallel to the strobe input pin 1 of each shift/storage register. With the output enable pin, pin 15, of each register tied high to +5 Vdc, the positive-going strobe pulse at input pin 1 transfers data in the shift registers through their respective storage registers to output pins 4, 5, 6, 7, 14, 13, 12, and 11. The data, at the output pins of the registers, are used as control signals for the associated assembly or circuit.

The data output from shift register U10, CL7 through CL0, are synthesizer coarse loop control bits which are input to input pins 1 through 8 of connector P2 of coarse loop assembly A1A2. These control bits, along with bits CL9 and CL8 from U11 to input pins 10 and 11, are input to programmable counters U7, U8, and U9 (Figure 7-15) where they establish a preset condition, or number, for terminal count. These ten data bits are the last ten bits of the data input clocked into the control register prior to the positive-going strobe pulse at input pin 1 of each shift register.

The data output from shift register U11, in addition to data bits CL8 and CL9 previously described, are band switch bits BS1 and BS0 and fine loop bits FL10 through FL7. Band switch bits BS1 and BS0 are output from pins 6 and 7 of U11 and are applied to input pins 12 and 13 of connector P2 of coarse loop assembly A1A2 and to input pins 6 and 7 of connector P1 of main loop assembly A1A3. They control the band switching function of the local oscillator. Fine loop bits FL10 through FL7 are output from pins 14 through 11 and are applied to input pins 17 through 14 of connector P1 of fine loop assembly A1A1. These control bits, along with bits FL6 through FL0 from shift register U12 to input pins 13 through 7, are input to programmable counters U5 through U7 where they establish a preset condition, or number, for terminal count.

The data output from shift register U8 are attenuator control bits AT2 through AT0 and manual gain control bits MG4 through MG0. Attenuator control bits AT2 through AT0 are output from pins 4 through 6 of U8 and are applied to input pins 17 through 15 of attenuator control assembly A1A5. These three control bits are input to AGC/MAN select switch U3,

on A1A5 (Figure 7-18), where they help determine what combination of attenuator pads are to be placed on-line in the baseband signal input path. Manual gain control bits MG4 through MG0 are output from pins 7 through 11 of U8 and are applied to input pins 5 through 9 of digital-to-analog converter U9 as described in paragraph 4.5.2.6.

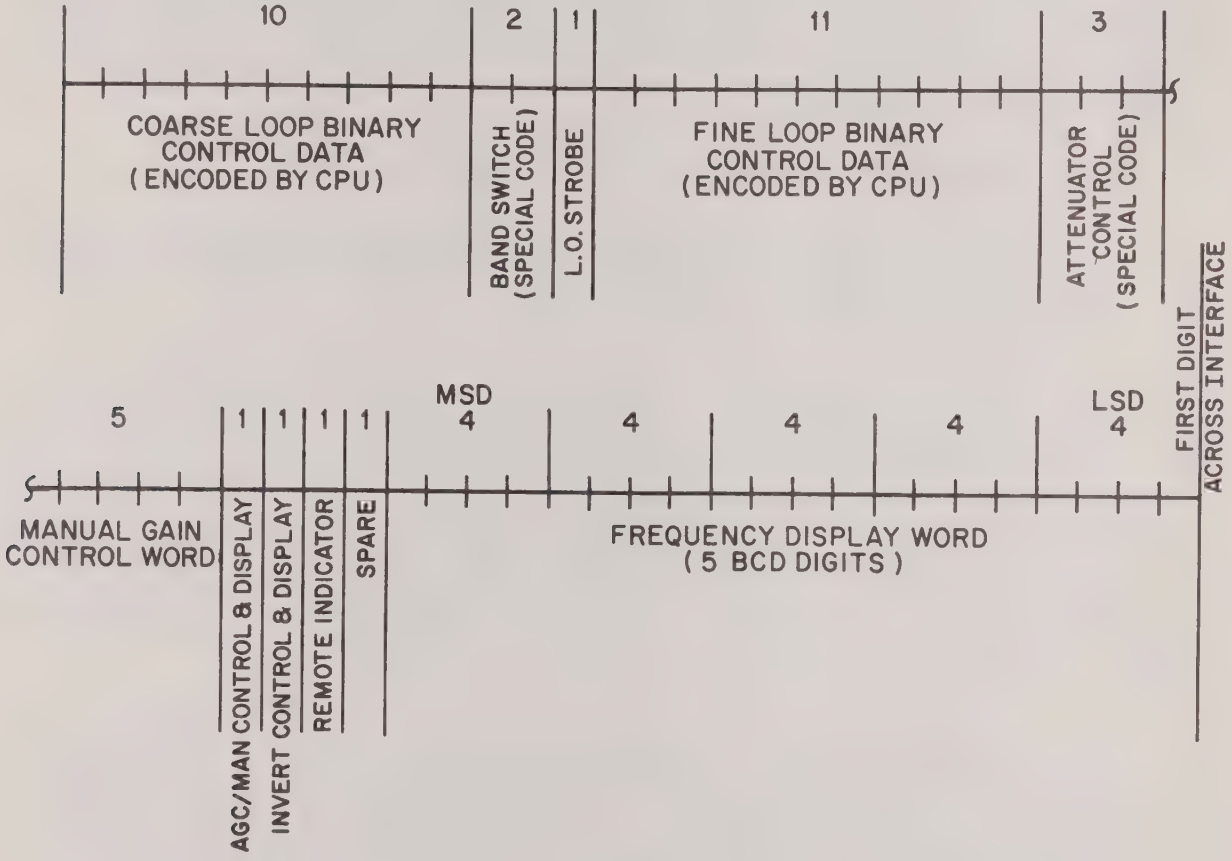


Figure 4-17. Serial Data Format

The data output from shift register U6 are the AGC/MAN control and display bit AGC, the invert control and display bit INV, remote indicator bit REM, and MSD control bits D3 through D0 of the frequency display word. The AGC, INV, and REM bits are output from pins 4 through 6 of U6 and are applied to input pins 11, 1, and 5 of driver U7, which is described in paragraph 4.5.2.3. Control bits D3 through D0 are output from pin 14 through 11 and are fed through pins 19, 17, 15, and 21 of connector J1 to input pins 6, 2, 1, and 7 of display driver U7 on display driver assembly A2A1. The remaining four digits of the frequency display word on the data stream are input to 8-bit shift registers U1 and U2 on the display driver assembly.

4.5.2.3 Driver U7

Refer to Figure 4-18 as an aid in the following description.

The AGC, INV, and REM outputs from shift register U6 and the ACTIVE output from NAND gate U2D are input to input pins 11, 1, 5, and 13 of driver U7. The high AGC input to U7 is inverted and is output as a low at output pin 10. The low I AGC output is fed through

pin 24 of connector J1, through display driver assembly A2A1 to pin 2 of connector 16 and to indicator DS11 on display board assembly A2.

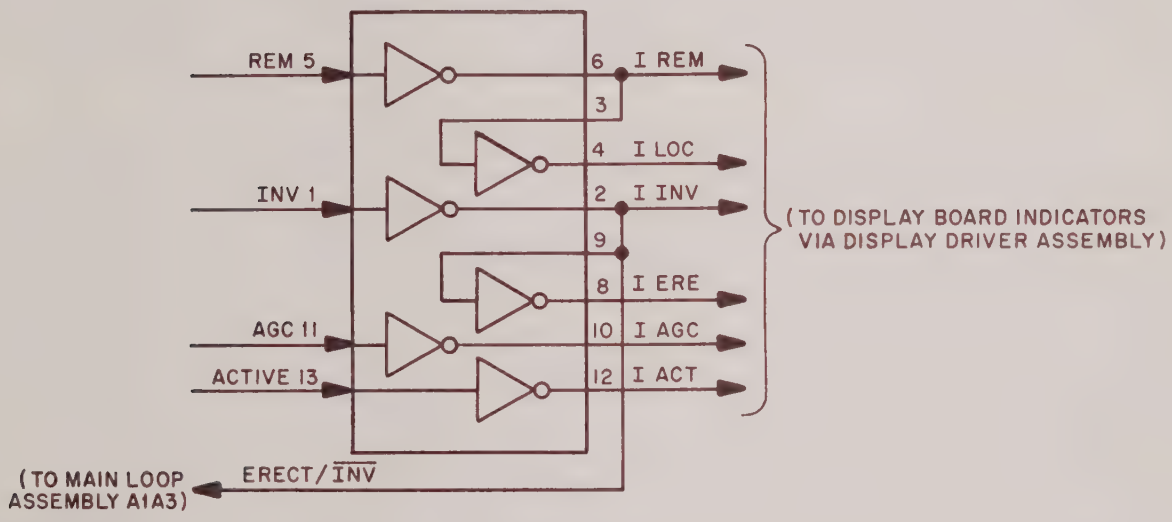


Figure 4-18. Driver U7 Functional Diagram

The high INV input to U7 is inverted and is output as a low at output pin 2. The low at output pin 2 is applied to the I INV line, input pin 9 of U7 and to input pin 7 of connector P1 of main loop assembly A1A3. The low applied to the I INV line is fed through pin 12 of connector J1, through display driver assembly A2A1 to pin 9 of connector J6 and to indicator DS8 on display board assembly A2. The low at input pin 9 is inverted and output as a high at output pin 8. The high I ERE is fed through pin 11 of connector J1, through display driver assembly A2A1 to pin 8 of connector J6 and to indicator DS9. With a high input, indicator DS9 does not light. Conversely, a low INV input to U7 presents a high input to indicator DS8 turning it off, if on, and a low input to indicator DS9, causing it to light.

The high REM input to U7 is inverted and is output as a low at output pin 6. The low at output pin 6 is applied to the I REM line and to input pin 3 of U7. The low applied to the I REM line is fed through pin 7 of connector J1, through display driver assembly A2A1 to pin 11 of connector J6 and to indicator DS6 on display board assembly A2. The low at input pin 3 is inverted and output as a high at output pin 4. The high I LOC is fed through pin 10 of connector J1, through display driver A2A1 to pin 10 of connector J6 and to indicator DS7. With a high input, indicator DS7 does not light. Conversely, a low REM input to U7 presents a high to indicator DS6 turning it off, if on, and a low input to indicator DS7, causing it to light.

The high ACTIVE input to U7 from NAND gate U2D, described in paragraph 4.5.2.4, is inverted and is output at pin 12. The low at output pin 12 is fed through pin 23 of connector J1, through display driver assembly A2A1 to pin 3 of connector J6 and to indicator DS10.

4.5.2.4 Logic Gates U1 and U2

During power-up, data from the CPU in the control unit are applied to all four demodulator units but only demodulator unit one receives the independent clock pulse, which, upon receipt of the strobe pulse to all four units, allows it to display the selected data. The CPU now outputs independent clock pulses and strobe pulses which resets the active latches of all four units. Next, the CPU outputs demodulator unit two data to all four units, but only unit two receives the independent clock pulse, allowing it to display selected data. The cycle repeats itself until all four demodulator units are set to the selected frequencies. During operation, when existing data to a demodulator unit is to be changed, strobe pulses are input to all units but only the selected demodulator unit receives its unique clock pulse allowing it to go active.

The independent clock pulse, which selects the active demodulator unit, is input to the selected demodulator unit motherboard via input pin 5 of connector P1. This positive-going pulse is applied to input pins 1 and 2 of NAND gate U2A. The negative-going output from U2A is inverted by inverter U1D, resulting in a positive-going pulse being applied to input pins 14 of NAND gate U1F and to input pin 5 of NAND gate U2B. The high input to pin 14, along with a normal high input to input pin 15 of U1F, result in a low output applied to input pin 12 of inverter U1E and to input pin 13 of NAND gate U2D. The high output from U1E is applied to the clock input pin of the shift registers of the demodulator unit. The high output from U2D is applied to input pin 9 of NAND gate U2C and to pin 13 of driver U7 which causes active control indicator DS10 to light. The normal high input on pin 6 of NAND U2B and the high output from inverter U1D to input pin 5 result in a low output from U2B. This low applied to input pin 8 of U2C, along with the high output from U2D to input pin 9, result in a high output from U2C. The high output from U2C is applied to input pin 12 of U2D, resulting in a high output from U2D until a positive-going strobe pulse is input to the demodulator unit at the same time a clock pulse is input to the demodulator unit.

The positive-going strobe pulse is input to pin 7 of connector P1 from the control unit. It is inverted by inverter U1B and applied to input pin 2 of inverter U1A, input pin 15 of NAND gate U1F, and to input pin 6 of NOR gate U1C. The high output of U1A is applied to the strobe input pins of the shift registers of the demodulator unit and to input pin 6 of NAND gate U2B. The high input to NAND gate U2B has no effect unless it arrives at the same time as a high clock pulse at input pin 14, which would result in the high active output line from U2D going low. The low input to input pin 6 NOR gate U1C has no effect unless it arrives at the same time as a low input at input pin 7. A negative-going pulse is output from output pin 4 of shift register U12. With a negative-going output from output pin 4 of U12 and the low input at pin 6 of U1C, the output from pin 5 of U1C goes high, supplying the LO strobe to input pin 14 of the synthesizer main loop.

4.5.2.5 2 MHz Reference Buffer U4

The 2 MHz reference input signal from reference generator assembly A3A1, described in paragraph 4.3.6, is applied to input pins 4 and 5 of buffer U4A and input pins 9 and 10 of amplifier U4B. With its positive voltage input pin, pin 5, tied to +5 Vdc, U4A converts the input signal to TTL levels for use as a clock input for synchronous 4-bit counter U1 of the synthesizer coarse loop. Amplifier U4B lowers the voltage levels of the input signal. The 2 MHz sine-wave output from U4B is filtered and shaped by the associated capacitors and inductors and is output to product detector U1 on IF demodulator assembly A1A6.

4.5.2.6 Digital-to-Analog Converter U9, Amplifier U5

Binary encoded manual gain data from the 5-bit manual gain control word in the data input to 8-bit shift register U8, described in paragraph 4.5.2.2, is input to digital-to-analog converter U9 via five data lines MG0 to MG4. The coded input, from 00000 to 11111, is converted into an analog voltage, from 0 Vdc to -5 Vdc, in 32 increments and output to amplifier U5. Resistor R22 provides full scale adjustment of the output from U5. The manual gain analog output from U5 is fed through switch U6 on attenuator control assembly A1A5 to gain-controlled amplifier Q1 and IF demodulator assembly A1A6.

4.5.2.7 Type 796064 Coarse Loop Assembly (A1A2)

Refer to Figure 4-19 for the functional block diagram and Figure 7-15 for the schematic diagram of Coarse Loop Assembly A1A2. Inputs to the coarse loop are the 2 MHz reference input, ERECT/$\overline{\text{INV}}$, BS1 and BS0, and the coarse loop data, CL0 through CL9. The 2 MHz reference input signal is input to the coarse loop via input pin 17 of connector J1 from reference buffer U4A on the motherboard assembly as described in paragraph 4.5.2.5. It is then applied to input pin 2 of U1 of divide-by-20/25 counters U1, U4A. The ERECT/$\overline{\text{INV}}$ data bit is input to the coarse loop via input pin 7 of connector J1 from driver U7 on the motherboard assembly as described in paragraph 4.5.2.3. As an erect bit, it is a high level which is applied input pin 1 of NAND gate U2A of decode logic U2A, U2B, U2D. The BS1 and BS0 band switch data bits are input to the coarse loop via input pins 12 and 13 of connector P2 from output pins 6 and 7 of 8-bit shift register U11 on the motherboard assembly as described in paragraph 4.5.2.2. Data bits BS1 and BS0 are binary encoded inputs which are applied to the bases of band switch switches Q2 and Q3. The coarse loop data bits are input to the coarse loop via input pins 1 through 11, CL0 through CL9, of connector P2 from the outputs of 8-bit shift registers U10 and U11 on the motherboard assembly. Data bits CL0 through CL9 are binary encoded inputs which are applied to the inputs of divide-by-Np programmable counters U7, U8, and U9.

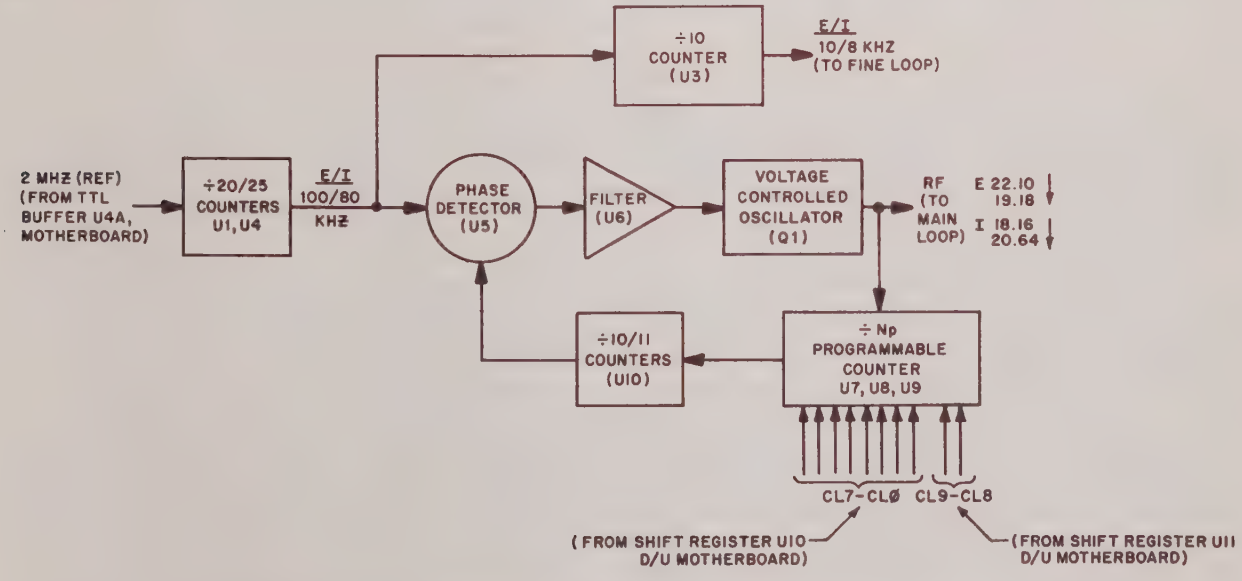


Figure 4-19. Coarse Loop Assembly Simplified Block Diagram

Outputs from the coarse loop are a 10/8 kHz output, INV/$\overline{\text{UPR}}$, UPR/$\overline{\text{INV}}$, and RF signals in two frequency ranges; 22.10 MHz down to 19.18 MHz in the erect mode and 18.16 MHz up to 20.64 MHz in the invert mode. In the erect mode, the 10 kHz output signal is output from output pin 4 of connector P1. It is then applied to fine loop input pin 4 of connector P1 and to input pin 1 of mixer U1. In the invert mode, the 8 kHz output signal follows the same route described for the 10 kHz output signal. The high INV/$\overline{\text{UPR}}$ output from output pin 5 of connector P1 is applied to fine loop input pin 5 of connector P1 and to main loop input pin 5 of connector P2. The high UPR/$\overline{\text{INV}}$ output from output pin 6 of connector P1 is applied to fine loop input pin 6 of connector P1 and to main loop input pin 4 of connector P2. The two ranges of RF signals are output from pin 14 of connector P2 and applied to main loop input 3 of connector P2.

The high ERECT/$\overline{\text{INV}}$ input decoder logic U2A, U2B, U2D, after decoding, causes divide-by-20/divide-by-25 counters U1 and U4A to divide the 2 MHz reference input by 20 in the erect mode. The 100 kHz output from U4A is applied to divide-by-10 counter U3, where it is divided by 10, and to the input of phase detector U5, where it provides a reference frequency. The 10 kHz output from U3 is applied to fine loop phase detector U1, where it provides a reference frequency. A low ERECT/$\overline{\text{INV}}$ input, or invert mode data bit, causes the 2 MHz reference input to be divided by 25 with the 80 kHz output following the route described for the 100 kHz output.

The 100/80 kHz input to phase detector U5 is compared to the input from programmable counters U7, U8, and U9 and the two-modulus prescaler, divide-by-10/divide-by-11 counter U10. With no change in the two inputs to U5, the output to filter U6 and VCO Q1 remains unchanged. As a result, the RF output from the coarse loop to the main loop remains unchanged.

A change to the coarse loop data, which results from a change of status at the control unit, results in a change of the divide-by-number ($\div$N) in counters U7 through U10. The new output from the programmable counters is detected by phase detector U5 which adjusts its output either up or down accordingly. As a result, the VCO output to the main loop is changed.

4.5.2.7.1 Decoder Logic U2A, U2B, U2D and Divide-by-Counters U1, U4A

A high on the ERECT/$\overline{\text{INV}}$, pin 7 of connector P1, from line driver U7 on the motherboard causes the coarse loop to operate in the erect mode in the following manner. With input pins 12 and 13 of NAND gate U2D tied low to ground, the output of U2D is high. This high is applied to input pin 2 of NAND gate U2A, input pin 5 of NAND gate U2B, and to input pin 5 of counter U1. The high to input pin 5 of U1 sets a count of four into U1. A high input at input pin 7 of connector P1 is applied to input pin 1 of NAND gate U2A. This high, along with the high output from U2D, results in a low output pin 3. The low output at pin 3 of U2A is applied to INV/$\overline{\text{UPR}}$ output pin 5 of connector P1 and to input pins 4 and 3 of counter U1 which count as zeros on the 2^1 and 2^0 inputs.

Refer to Figure 4-20. The low output from U2A, when applied to input pin 4 of NAND gate U2B along with the constant high input to pin 5 of U2B, results in a high output at pin 6 of U2B. This high output is applied to the UPR/$\overline{\text{INV}}$ output pin 6 of connector P1 and to input pin 6 of counter U1. The high to input pin 6 of U1 adds a 2^3, or eight, to the four set into the counter. Counter U1 now begins to count down from 12. The output at output pin 15 of U1 goes high at count 15 for one count. This high is applied to input pin 10 of NAND gate U2C which results in a low output from pin 8 to LOAD input pin 9 of U1, enabling U1 to load at count 12. At count 12, the output at pin 15 of U1 goes low resulting in a low input to CLK input pin 1 of U4A. This negative-going transition at input pin 1 causes U4A to change states, the high output at $\overline{Q}$ pin 6 goes low, and, conversely, the Q output at pin 5 goes high.

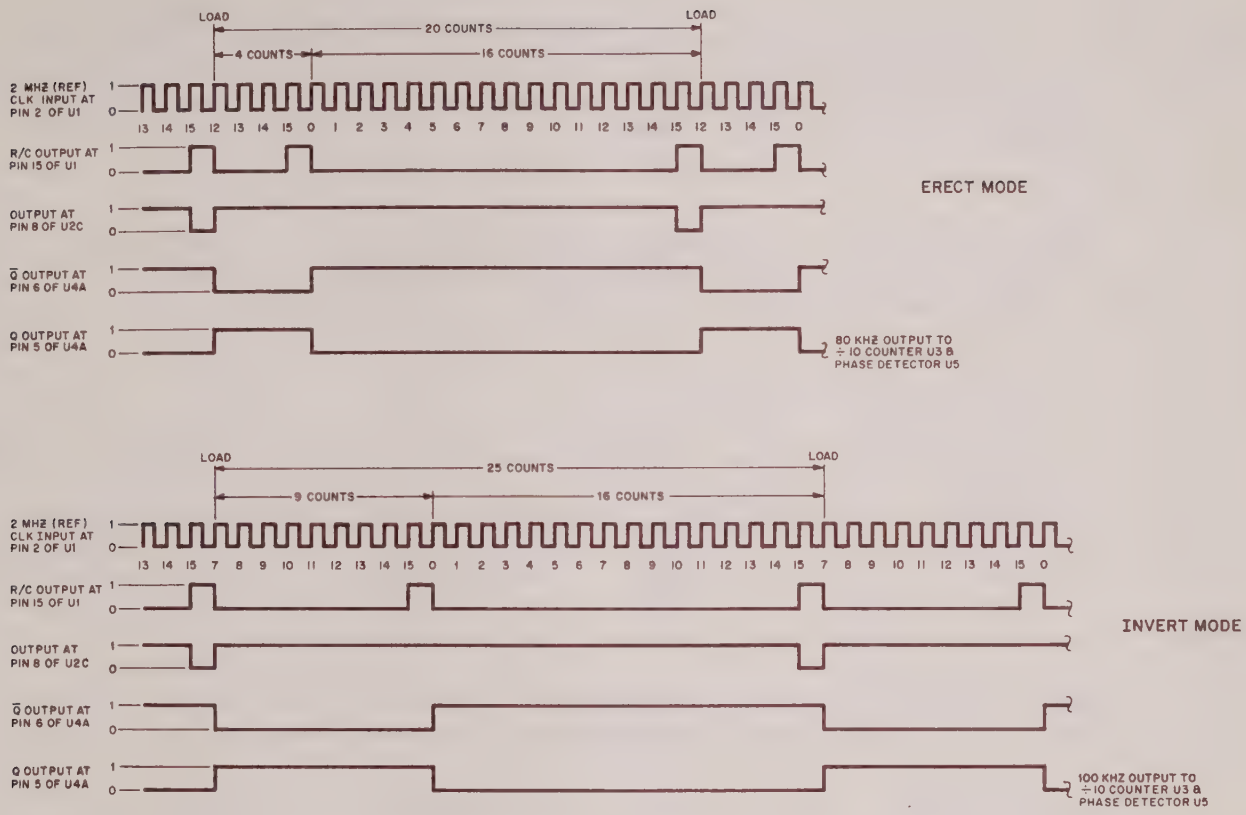

LOAD
20 COUNTS
LOAD
4 COUNTS
16 COUNTS
2 MHZ (REF) CLK INPUT AT PIN 2 OF U1
13 14 15 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 12 13 14 15 0
R/C OUTPUT AT PIN 15 OF U1
OUTPUT AT PIN 8 OF U2C
Q̄ OUTPUT AT PIN 6 OF U4A
Q OUTPUT AT PIN 5 OF U4A
ERECT MODE
80 KHZ OUTPUT TO ÷ 10 COUNTER U3 & PHASE DETECTOR U5
LOAD
25 COUNTS
LOAD
9 COUNTS
16 COUNTS
2 MHZ (REF) CLK INPUT AT PIN 2 OF U1
13 14 15 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 7 8 9 10 11 12 13 14 15 0
R/C OUTPUT AT PIN 15 OF U1
OUTPUT AT PIN 8 OF U2C
Q̄ OUTPUT AT PIN 6 OF U4A
Q OUTPUT AT PIN 5 OF U4A
INVERT MODE
100 KHZ OUTPUT TO ÷ 10 COUNTER U3 & PHASE DETECTOR U5

Figure 4-20. Divide-by-Counters U1, U4A Timing

The low output at pin 15 of U1 is also applied to input pin 10 of NAND gate U2C which, along with the low from pin 6 of U4A, results in a high output at pin 8 to LOAD input pin 9 of U1. With ENP pin 7 and ENT pin 10 held high from output pin 11 of NAND gate U2D, the high at LOAD input pin 9 causes U1 to begin its count to 15. At count 15, the output at pin 15 goes high for one count. At count 0, the output at pin 15 goes low. Again, this negative-going transition at input pin 1 causes U4A to change states.

In the Invert Mode, a low on the ERECT/$\overline{\text{INV}}$ line from driver U7 on the motherboard is applied to input pin 1 of NAND gate U2A. This low, along with the high at input pin 2 from output pin 11 of U2D, results in a high output at pin 3. This high is applied to input pin 4 of NAND gate U2B, INV/$\overline{\text{UPR}}$ output pin 5 of connector P1, and to input pins 4 and 3 (2^1 and 2^0) of U1. The high at input pin 4 of U2B, along with the high at input pin 5 from output pin 11 of U2D, results in a low output at pin 6 which is applied to UPR/$\overline{\text{INV}}$ output pin 6 of connector P1 and to input pin 6 (2^3) of U1. With input pin 6 (2^3) low, input pin 5 (2^2) high, and input pins 4 and 3 (2^1 and 2^0) high, U1 now counts down from 7. With a count of 7, the total counts between load points increases by 5 for a total of 25.

4.5.2.7.2 Phase Detector U5

The 100 kHz (Erect Mode) or 80 kHz (Invert Mode) output from pin 5 of U4A is input to the reference frequency (RF) input pin 1 of phase detector U5. Phase detector U5 compares the relative timing of the negative-going transitions of the variable frequency (VF)

input at pin 3 from programmable counters U7, U8, and U9 against the reference frequency input at pin 1. When it detects a difference, it generates either an UP signal at output pin 13 or a DOWN signal at output pin 2, whose duration is equal to the RF - VF timing difference. The outputs at pins 13 and 2 are normally high. When an UP signal is generated, the output at pin 13 drops low. This low is input to filter U6 at input pin 2.

4.5.2.7.3 Filter U6

Filter U6 is a standard operational amplifier. Input pin 2 is its inverting input and input pin 3 is its non-inverting input. With an UP signal generated by phase detector U5, the input at input pin 2 is low, resulting in a high output at pin 6 which increases the voltage to voltage-controlled oscillator Q1.

4.5.2.7.4 Voltage-Controlled Oscillator Q1

In the Erect Mode, voltage-controlled oscillator Q1 tunes from 22.10 MHz for a demodulator frequency of 000.00 kHz (Table 4-1) down to 19.10 MHz for a demodulator frequency of 308.00 kHz. In the Invert Mode, VCO Q1 tunes from 18.16 MHz for a demodulator frequency of 000.00 kHz (Table 4-2) to 20.64 MHz for a demodulator frequency of 308.00 kHz. The output from VCO Q1 is applied past bandswitch switches Q2 and Q3 to buffer amplifier Q4.

4.5.2.7.5 Bandswitch Switches Q2 and Q3

Bandswitch switches Q2 and Q3 limit the VCO frequency output to four bands with an approximate 1.4 MHz bandwidth. The bands and their respective frequency limits are listed in Table 4-3.

Table 4-1. Coarse Loop Assembly - Synthesizer Data (Erect Mode)

Demodulator Frequency (kHz)	Coarse Loop Data Bits			÷N	Bandswitch Bits		Coarse Loop Frequency (MHz)	LO Frequency (MHz)
	U9	U8	U7					
	9 8	7 6 5 4	3 2 1 0		1	0		
0 0 0 . 0 0	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	2 . 0 0 0 0 0
0 0 0 . 0 1	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 9 9 9
0 0 0 . 0 2	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 9 9 8
0 0 0 . 9 9	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 9 0 1
0 0 1 . 0 0	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 9 0 0
0 0 1 . 0 1	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 8 9 9
0 0 9 . 9 9	1 0	0 0 1 1	1 0 1 0	2 2 1	1	1	2 2 . 1 0	1 . 9 9 0 0 1
0 1 0 . 0 0	1 0	0 0 1 1	1 0 0 1	2 2 0	1	1	2 2 . 0 0	1 . 9 9 0 0 0
0 2 0 . 0 0	1 0	0 0 1 1	1 0 0 0	2 1 9	1	1	2 1 . 9 0	1 . 9 8 0 0 0
0 9 9 . 9 9	1 0	0 0 1 1	0 0 0 1	2 1 2	1	1	2 1 . 2 0	1 . 9 0 0 0 1
1 0 0 . 0 0	1 0	0 0 1 0	1 0 1 0	2 1 1	1	0	2 1 . 1 0	1 . 9 0 0 0 0
1 0 3 . 0 0	1 0	0 0 1 0	1 0 1 0	2 1 1	1	0	2 1 . 1 0	1 . 8 9 7 0 0
1 1 0 . 0 0	1 0	0 0 1 0	1 0 0 1	2 1 0	1	0	2 1 . 0 0	1 . 8 9 0 0 0
1 2 0 . 0 0	1 0	0 0 1 0	1 0 0 0	2 0 9	1	0	2 0 . 9 0	1 . 8 8 0 0 0
1 3 0 . 0 0	1 0	0 0 1 0	0 1 1 1	2 0 8	1	0	2 0 . 8 0	1 . 8 7 0 0 0
2 4 9 . 9 9	1 0	0 0 0 1	0 1 0 0	1 9 7	1	0	1 9 . 7 0	1 . 7 5 0 0 1
2 5 0 . 0 0	1 0	0 0 0 1	0 1 0 1	1 9 6	0	1	1 9 . 6 0	1 . 7 5 0 0 0
3 0 8 . 0 0	1 0	0 0 0 0	1 0 1 0	1 9 1	0	1	1 9 . 1 0	1 . 6 9 2 0 0

Table 4-2. Coarse Loop Assembly - Synthesizer Data (Invert Mode)

Demodulator Frequency (kHz)	Coarse Loop Data Bits U9	U8	U7	÷ N	Bandswitch Bits 1	0	Coarse Loop Frequency (MHz)	LO Frequency (MHz)
	9 8	7 6 5 4	3 2 1 0					
000.00	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00400
000.01	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00401
000.02	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00402
000.99	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00499
001.00	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00500
001.01	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00501
003.50	1 0	0 1 0 0	0 1 1 0	2 2 7	0	1	18.16	2.00750
003.51	1 0	0 1 0 0	0 1 1 1	2 2 8	0	1	18.24	2.00751
003.52	1 0	0 1 0 0	0 1 1 1	2 2 8	0	1	18.24	2.00752
009.99	1 0	0 1 0 0	0 1 1 1	2 2 8	0	1	18.24	2.01399
010.00	1 0	0 1 0 0	0 1 1 1	2 2 8	0	1	18.24	2.01400
013.50	1 0	0 1 0 0	0 1 1 1	2 2 8	0	1	18.24	2.01750
023.50	1 0	0 1 0 0	1 0 0 0	2 2 9	0	1	18.32	2.02750
183.50	1 0	0 1 1 0	0 1 0 0	2 4 5	0	1	19.60	2.18750
183.51	1 0	0 1 1 0	0 1 0 1	2 4 6	1	0	19.68	2.18751
308.00	1 0	0 1 1 1	0 1 1 1	2 5 8	1	0	20.64	2.31200

Table 4-3. VCO - Bandswitch Frequency Data

Erect Mode				Invert Mode			
Bandswitch Bits		VCO Frequency Limits		Bandswitch Bits		VCO Frequency Limits	
1	0	FROM	TO	1	0	FROM	TO
1	1	21.20	22.10	1	1	(Not used)	
1	0	19.70	21.10	1	0	19.68	21.04
0	1	19.10	19.60	0	1	18.16	19.60
0	0	(Not used)		0	0	(Not used)	

With a high input on BS1, pin 12 of connector P2, transistor Q2 conducts adding inductor L2 in parallel to transformer T1. With transformer T1 and capacitor C12 providing the tank circuit for Q1, the adding of L2 in parallel to T1 reduces the inductance in the tank circuit, effectively shortens the transmission line from Q2, and increases the output frequency. The output from Q1 is applied to buffer amplifier Q4. The 18.16 MHz to 22.10 MHz output from Q4 is applied to pin 14 of connector P2 and to clock input pin 1 of prescaler U10.

4.5.2.7.6 Two-Modulus Prescaler U10

The 16.70 MHz to 22.10 MHz output from buffer amplifier Q4 is applied to divide-by-10/11 counter U10 at clock (CLK) input pin 1. Counter U10 divides the input at pin 1 by 10 when the input at pin 2 ($\overline{\text{PE 1}}$) is high and conversely, it divides by 11 when the input at pin 2 is low. The level at input pin 2 is determined by the MAX/MIN output from pin 12 of counter U7. The divided by 10 or 11 output from TTL output pin 11 of U10 is applied to the clock inputs of counters U7, U8, and U9.

4.5.2.7.7 Programmable Counters U7, U8, and U9

Programmable counters U7, U8, and U9, along with U10 described in paragraph 4.5.2.7.6, determine the variable frequency input to phase detector U5 described in paragraph 4.5.2.7.2. With $\overline{U}$/D input pin 5 of U7 tied high, and U/$\overline{D}$ input pin 10 of both U8 and U9 tied to ground, all three counters are limited to counting down.

Refer to Figure 4-21 for the following description. For the purpose of explanation refer to the last entry in the Coarse Loop Data Bits column of Table 4-1. From the table, the coarse loop divide-by-N number for a coarse loop data input of 10 0000 1010 is 191. This input is equivalent to decimal inputs of 2 to U9, 0 to U8, and 10 to U7. The formula for divide-by-N for the coarse loop is:

$$\div N = 160\,(U9 - 1) + 10\,(U8 + 2) + U7 + 1$$

substituting:

$$\div N = 160\,(1) + 10\,(2) + 10 + 1$$

$$\div N = 191$$

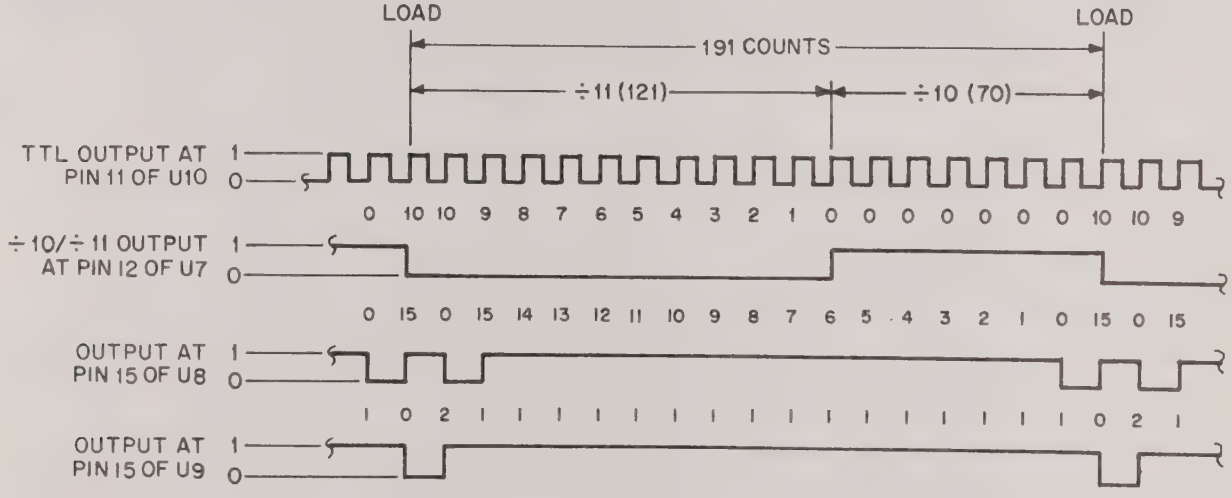


Figure 4-21. Divide-By-Counters U7, U8, U9, and U10, Typical ÷191

The TTL output from pin 11 of U10 is applied to the clock inputs of counters U7, U8, and U9. With the R/C output of U8 tied to the EN$\overline{P}$ input of U9, the clock input to U9 is enabled when the output of U8 goes low. With the coarse loop data input to U8 at 0000, the output from U8 goes low at 0 for one clock pulse and then goes high. This high output from U8 causes the output from U9 to go low. With R/C output pin 15 of U9 tied to the LOAD input pins of U7, U8, and LOAD pin 9, MIN/MAX output from pin 12 of U7 goes low and counter U10 starts to divide by 11. The low input at LOAD input pin 9 of U8 causes U8 to count two counts while counter U9 counts from 0 to 2. At 2, the output from pin 15 of U9 goes high.

Counter U7 started counting from 10 upon receipt of the low input at LOAD pin 11. The output at pin 12 is now held low, causing counter U10 to divide-by-11, until it counts down to 0 at which time the output goes high causing U10 to divide-by-10.

When the output from pin 15 of U9 went high, counter U8 started counting down from 15 to 0. At 0, the output from U8 goes low until it receives the positive-going pulse from pin 11 of counter U10. At this point the cycle repeats itself until the coarse loop data input changes. The output from VCO Q1 is applied to the main loop assembly, described in paragraph 4.5.2.9, where it is used with the input from the fine loop assembly, described in paragraph 4.5.2.8, to establish the desired local oscillator frequency for the demodulator unit.

4.5.2.8 Type 796063 Fine Loop Assembly (A1A1)

Refer to Figure 4-22 for the functional block diagram and Figure 7-14 for the schematic diagram of Fine Loop Assembly A1A1. Inputs to the fine loop are a 10/8 kHz reference input, INV/$\overline{\text{UPR}}$, UPR/$\overline{\text{INV}}$, and the fine loop data bits, FL0 through FL10. The 10/8 kHz reference input signal is input to the fine loop via input pin 4 of connector P1 from counter U3 on the coarse loop assembly as described in paragraph 4.5.2.7. The INV/$\overline{\text{UPR}}$ level is input via pin 5 of connector P1 from pin 3 of NAND gate U2A on the coarse loop assembly, described in paragraph 4.5.2.7.1. The UPR/$\overline{\text{INV}}$ level is input via pin 6 of connector P1 from pin 6 of NAND gate U2B described in paragraph 4.5.2.7.1. Fine loop data bits are input to the fine loop via input pins 7 through 17, FL0 through FL10, of connector P1 from the outputs of 8-bit shift registers U11 and U12 on the motherboard assembly. Data bits FL0 through FL10 are binary encoded inputs which are applied to the inputs of divide-by-Np programmable counters U5, U6, and U7.

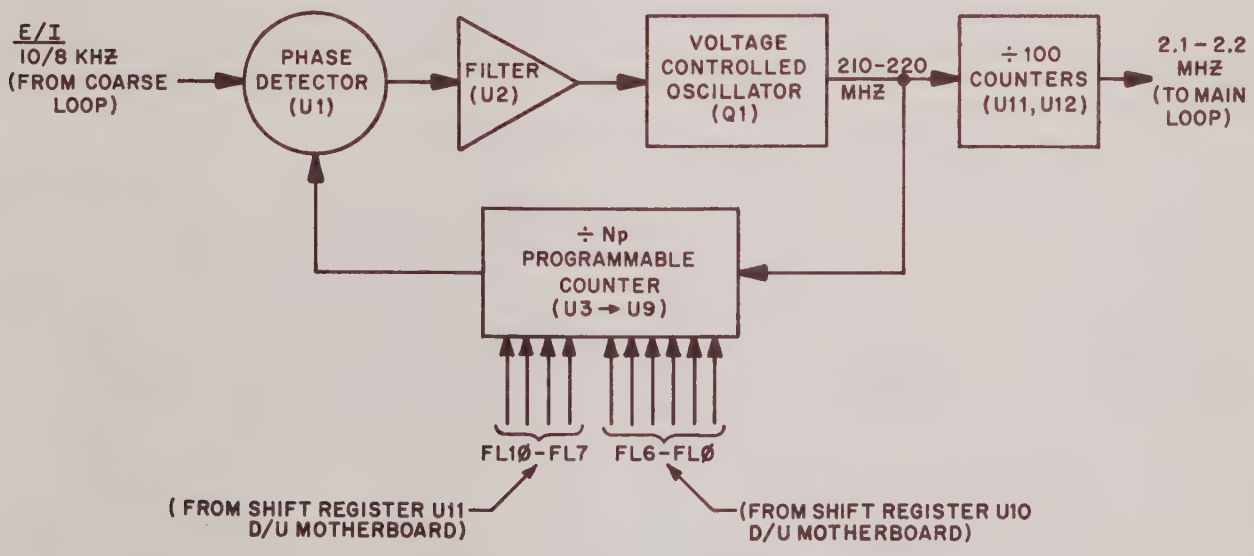


Figure 4-22. Fine Loop Assembly Simplified Block Diagram

Outputs from the fine loop are RF signals in two frequency ranges; 2.1000 MHz up to 2.1999 MHz in the erect mode and 2.1799 MHz down to 2.1000 MHz in the invert mode.

The 10/8 kHz input to phase detector U1 is compared to the input from programmable counters U3 through U9. With no change in the two inputs to U1, the output to filter U2 and VCO Q1 remains unchanged. As a result, the RF output from the fine loop to the main loop remains unchanged.

A change to the fine loop data, which results from a change of status at the control unit, results in a change of the divide-by-number (N) in counters U5, U6, and U7. A change in upright or inverted status, which results from a change of status at the control unit and is decoded by the decoder logic on the coarse loop and then applied to the fine loop, affects the range of counters U3 and U4.

4.5.2.8.1 Phase Detector U1

The 10 kHz (Erect Mode) or 8 kHz (Invert Mode) output from pin 4 of coarse loop connector P1 is input to RF input pin 1 of phase detector U1 via pin 4 of fine loop connector P1. Phase detector U1 compares the relative timing of the negative-going transitions of the variable frequency input at pin 3 from programmable counters U3 through U9 against the reference frequency input at pin 1. When it detects a difference, it generates either an UP signal at output pin 13 or a DOWN signal at output pin 2 whose duration is equal to the RF - VF timing difference. The outputs at pins 13 and 2 are normally high. When an UP signal is generated, the output at pin 13 drops low. This low is applied to filter U2 at input pin 2. When a DOWN signal is generated, the output at pin 2 drops low and is applied to U2 at input pin 3.

4.5.2.8.2 Filter U2

Filter U2 is a standard operational amplifier. Input pin 2 is its inverting input and input pin 3 is its non-inverting input. With an UP signal generated by phase detector U1, the input at pin 2 is low resulting in a high output at pin 6 which increases the voltage to voltage-controlled oscillator Q1. A DOWN signal generated by U1 results in a decrease in voltage at output pin 6. This decreases the voltage to Q1.

4.5.2.8.3 Voltage-Controlled Oscillator Q1

In the Erect Mode, voltage-controlled oscillator Q1 tunes from 210.000 MHz for a demodulator frequency of 000.00 kHz (Table 4-4) up to 218.000 MHz for a demodulator frequency of 308.00 kHz. In the Invert Mode, VCO Q1 tunes from 212.800 MHz for a demodulator frequency of 000.00 kHz (Table 4-5) up to 214.400 MHz for a demodulator frequency of 308.00 kHz. The output from VCO Q1 is applied to buffer amplifier Q2. The output from Q2 via transformer T1 is applied to clock input pin 1 of divide-by-10 counter U11 and to clock input pin 1 of divide-by-10/11 counter U9 in the feed-back loop to phase detector U1.

4.5.2.8.4 Divide-By-10 Counter U11

With $\overline{Q4}$ output pin 9 tied to $\overline{PE\ 2}$ input pin 3, counter U11 divides the 210 MHz to 220 MHz input at clock input pin 1 by 10. The resultant 21 MHz to 22 MHz is output via TTL O/P pin 11 to CLK A input pin 10 of divide-by-10 counter U12.

4.5.2.8.5 Divide-By-10 Counter U12

With QA output pin 9 tied to input pin 11, counter U12 divides the 21 MHz to 22 MHz input at input pin 10 by 10. The resultant 2.10 MHz to 2.2 MHz is output via Q_D pin 8 and pin 1 of connector P2 to phase detector U1 of the main loop assembly described in paragraph 4.5.2.9.

Table 4-4. Fine Loop Assembly - Synthesizer Data (Invert Mode)

Demodulator Frequency (kHz)	Fine Loop Data Bits U5 10 9 8 7	U6 6 5 4	U7 3 2 1 0	÷N	Fine Loop Frequency (MHz)	LO Frequency (MHz)
000.00	1000	000	0000	26600	212.800	2.00400
000.01	0111	110	0011	26599	212.792	2.00401
000.02	0111	110	0010	26598	212.784	2.00402
000.99	0111	000	0001	26501	212.008	2.00499
001.00	0111	000	0000	26500	212.000	2.00500
001.01	0110	110	0011	26499	211.992	2.00501
003.50	0100	011	0010	26250	210.000	2.00750
003.51	1110	011	0001	27249	217.992	2.00751
003.52	1110	011	0000	27248	217.984	2.00752
009.99	1000	000	0001	26601	212.808	2.01399
010.00	1000	000	0000	26600	212.800	2.01400
013.50	0100	011	0010	26250	210.000	2.01750
023.50	0100	011	0010	26250	210.000	2.02750
183.50	0100	011	0010	26250	210.000	2.18750
183.51	1110	011	0001	27249	217.992	2.18751
308.00	1010	000	0000	26800	214.400	2.31200

Table 4-5. Fine Loop Assembly - Synthesizer Data (Erect Mode)

Demodulator Frequency (kHz)	Fine Loop Data Bits U5 10 9 8 7	U6 6 5 4	U7 3 2 1 0	÷N	Fine Loop Frequency (MHz)	LO Frequency (MHz)
000.00	0000	000	0000	21000	210.00	2.00000
000.01	0000	000	0001	21001	210.01	1.99999
000.02	0000	000	0010	21002	210.02	1.99998
000.99	0000	110	0011	21099	210.99	1.99901
001.00	0001	000	0000	21100	211.00	1.99900
001.01	0001	000	0001	21101	211.01	1.99899
009.99	1001	110	0011	21999	219.99	1.99001
010.00	0000	000	0000	21000	210.00	1.90000
020.00	0000	000	0000	21000	210.00	1.98000
099.99	1001	110	0011	21999	219.99	1.90001
100.00	0000	000	0000	21000	210.00	1.90000
103.00	0011	000	0000	21300	213.00	1.89700
110.00	0000	000	0000	21000	210.00	1.89000
120.00	0000	000	0000	21000	210.00	1.88000
130.00	0000	000	0000	21000	210.00	1.87000
249.99	1001	110	0011	21999	219.00	1.75001
250.00	0000	000	0000	21000	210.00	1.75000
308.00	1000	000	0000	21800	218.00	1.69200

4.5.2.8.6 Divide-By-10/11 Counter U9

Divide-by-10/11 counter U9, in conjunction with divide-by-10 counter U8, acts as a two-modulus prescaler. The 210 MHz to 220 MHz input at clock input pin 1 is divided by either 10 or 11 dependent upon the level of the inputs at $\overline{PE\ 2}$ pin 3 and $\overline{PE\ 1}$ pin 2. If either input is high, U9 divides by 10. If both inputs are low, U9 divides by 11. The divided-by-10 or 11 output from TTL output pin 11 of U9 is applied to clock input pin 2 of divide-by-10 counter U8.

4.5.2.8.7 Divide-By-10 Counter U8

With U/$\overline{D}$ input pin 1 tied low, counter U8 counts down, or divides, the input at clock input pin 2 by 10. With input pins 12 and 13 of NAND gate U13D tied low, the output at pin 11 to input pin 10 of NAND gate U13C and to LOAD pin 9 of U8 is high. With LOAD pin 9 effectively tied high, the internal counter of U8 is enabled and the output at pin 15 goes low after 10 clock pulses. The output from pin 15 of U8 is applied to the clock inputs of programmable counters U3 through U7.

4.5.2.8.8 Programmable Counters U3 through U7

Programmable counters U3 through U7, along with counters U9 and U8, described in paragraphs 4.5.2.8.6 and 4.5.2.8.7, determine the variable frequency input to phase detector U1 described in paragraph 4.5.2.8.1. With each U/$\overline{D}$ input pin 1 of counters U3 through U7 tied low, all five counters are limited to counting down.

Refer to Figure 4-23 for the following description. For the purpose of explanation refer to the last entry in the Fine Loop Data Bits column of Table 4-5. From the table, the fine loop divide-by-N number for a fine loop data input of 1000 000 0000 is 21800. This input is equivalent to decimal inputs of 8 to U5, 0 to U6, and 0 to U7. The formula for divide-by-N for the fine loop in the erect mode is:

$$\div N = 21000 + 100\,(U5) + 16\,(U6) + U7,$$

substituting:

$$\div N = 21000 + 100\,(8) + 16\,(0) + 0,$$

$$\div N = 21800.$$

The formula for divide-by-N for the fine loop in the inverted mode is:

$$\div N = 25800 + 100\,(U5) + 16\,(U6) + U7.$$

In the erect mode, a low is input to pin 4 of U3 from pin 5 of coarse loop connector P1 via pin 5 of fine loop connector P1. A high is input to pin 3 of U3 and to pins 6, 5, and 3 of U4 from pin 6 of coarse loop connector P1 via pin 6 of fine loop connector P1. With pins 6 and 5 of U3 tied low, the decimal equivalent to U3 is a 1. With pin 4 of U4 tied low, the decimal equivalent to U4 is a 13. Conversely, in the inverted mode a high is input to pin 4 of U3 and a low is input to pin 3 of U3 and pins 6, 5, and 3 of U4. This results in, in the inverted mode, a decimal equivalent of 2 to U3 and 0 to U4.

The enable $\overline{P}$ (EN$\overline{P}$) inputs and the enable $\overline{T}$ (EN$\overline{T}$) inputs of counters U3 through U7 must be low to count. Any change at EN$\overline{P}$, EN$\overline{T}$, and LOAD has no effect on the operation of the counters until clocking occurs.

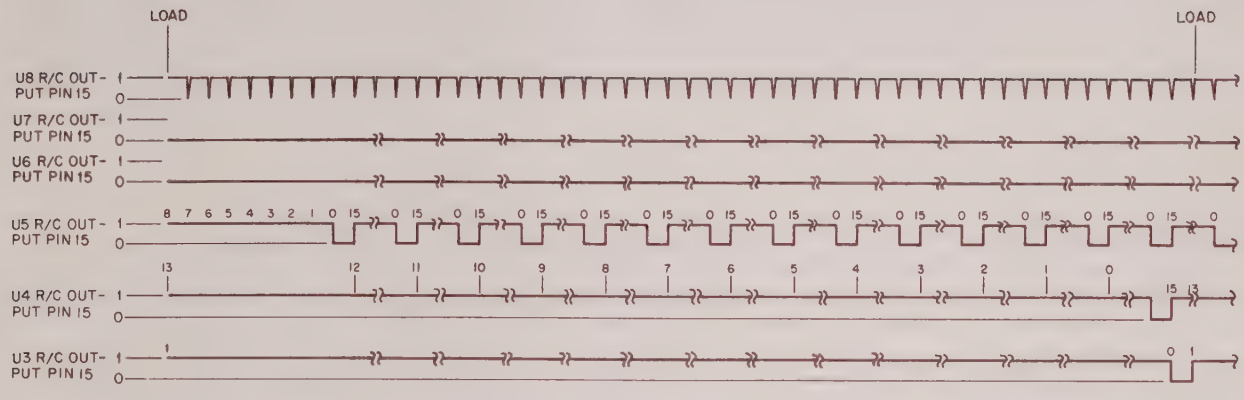


Figure 4-23. Divide-By-Counters U3 through U7, Typical ÷21800

Upon receipt of a positive-going transition at input pin 2, counter U5 starts to count down to 0 from 8. Upon receipt of each successive positive-going transition at input pin 2, U5 decrements, or counts down, one count. At count 0, the output at pin 15 of U5 goes low. The next positive-going transition causes U4 to decrement by one from 13 to 12. This cycle repeats itself until U4 decrements to 0 at which time the output at pin 15 of U4 goes low. The next positive-going transition causes U3 to decrement from 1 to 0.

4.5.2.9 Type 796062 Main Loop Assembly (A1A3)

Refer to Figure 4-24 for the functional block diagram and Figure 7-16 for the schematic diagram of Main Loop Assembly A1A3. Inputs to the main loop are RF signals in two frequency ranges from both the coarse loop and the fine loop, a local oscillator strobe pulse, BS1 and BS0, and UPR/$\overline{\text{INV}}$ and INV/$\overline{\text{UPR}}$ levels.

In the erect mode, RF inputs from the coarse loop are from 22.10 MHz down to 19.18 MHz and from the fine loop are from 2.1000 MHz up to 2.1999 MHz. In the invert mode, RF inputs from the coarse loop are from 18.16 MHz up to 20.64 MHz and from the fine loop are from 2.1799 MHz down to 2.1000 MHz. The LO STROBE pulse is input from NOR gate U1C, as described in paragraph 4.5.2.4. The BS1 and BS0 bandswitch data bits are input to the main loop via pins 6 and 7 of connector P1 from pins 6 and 7 of 8-bit shift register U11, as described in paragraph 4.5.2.2. The UPR/$\overline{\text{INV}}$ level is input via pin 4 of connector P2 from pin 6 of NAND gate U2B, described in paragraph 4.5.2.4. The INV/$\overline{\text{UPR}}$ level is input via pin 5 of connector P2 from pin 3 of NAND gate U2A described in paragraph 4.5.2.7.1.

The 2.1000 MHz to 2.1999 MHz input from the fine loop to phase detector U1 is compared to the IF output from mixer U6. The IF output from mixer U6 is a sum/difference frequency based on the 16.70 MHz to 22.56 MHz input from the coarse loop and the main loop VCO output frequency. As with the coarse loop and the fine loop, a change to the coarse loop data or fine loop data, which results from a change of status at the control unit, results in a

change in the inputs to the phase detector which, in turn, changes the main loop VCO output frequency and the resultant main loop output to input converter A1A4 described in paragraph 4.5.2.10.

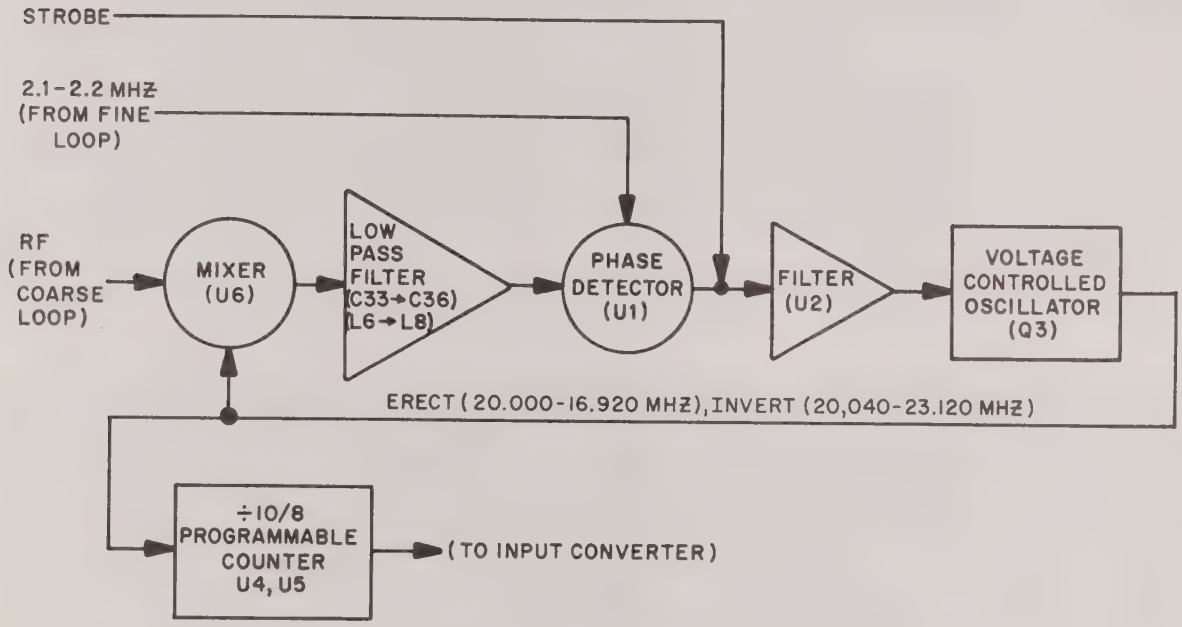


Figure 4-24. Main Loop Assembly Simplified Block Diagram

4.5.2.9.1 Phase Detector U1

The 2.1000 MHz to 2.1999 MHz (Erect Mode) or 2.1799 MHz to 2.1000 (Invert Mode) output from pin 1 of fine loop connector P1 is input to RF pin 1 of phase detector U1 via pin 1 of main loop connector P1. Phase detector U1 compares the relative timing of the negative-going transitions of the variable frequency input at pin 3 from IF output pin 4 of mixer U6 via the low-pass filter, amplifier, and shaper in its output circuit with the input at RF input pin 1. When it detects a difference, it generates either an UP signal at output pin 13 or a DOWN signal at output pin 2 whose duration is equal to the timing difference between the inputs at pins 3 and 1. The outputs at pins 13 and 2 are normally high. When an UP signal is generated, the output at pin 13 drops low. This low is input to filter U2 at input pin 2. When a DOWN signal is generated, the output at pin 2 drops low and is applied to U2 at input pin 3. During bandswitch changes to the main loop, a high LO STROBE input is applied to the base of Q1 of the strobe circuitry, composed of Q1 and Q2. The resultant output at pin D of Q2 pulls the DOWN line from U1 to U2 lower, ensuring that the main loop frequency is lower than the coarse loop frequency.

4.5.2.9.2 Filter U2

Filter U2 is a standard operational amplifier. Input pin 2 is its inverting input and input pin 3 is its non-inverting input. With an UP signal generated by phase detector U1, the input at pin 2 is low, resulting in a high output at pin 6 which increases the voltage to VCO Q3. A DOWN signal generated by U1 results in a decrease in voltage at output pin 6. This decreases the voltage to Q3.

4.5.2.9.3 Voltage-Controlled Oscillator Q3

In the Erect Mode, voltage-controlled oscillator Q3 tunes from 20.0000 MHz for a demodulator frequency of 000.00 kHz (Table 4-6) down to 16.9200 MHz for a demodulator frequency of 308.00 kHz. In the Invert Mode, VCO Q3 tunes from 16.032 MHz for a demodulator frequency of 000.00 kHz (Table 4-7) up to 18.496 MHz for a demodulator frequency of 308.00 kHz. The output from VCO Q3 is applied past bandswitch switches Q4 and Q5 to buffer amplifier Q6.

Table 4-6. Main Loop Assembly - Synthesizer Data (Erect Mode)

Demodulator Frequency (kHz)	Bandswitch Bits		Main Loop Frequency (MHz)	LO Frequency (MHz)
	1	0		
000.00	1	1	20.0000	2.00000
000.01	1	1	19.9999	1.99999
000.02	1	1	19.9998	1.99998
000.99	1	1	19.9901	1.99901
001.00	1	1	19.9900	1.99900
001.01	1	1	19.9899	1.99899
009.99	1	1	19.9901	1.99901
010.00	1	1	19.9900	1.99900
020.00	1	1	19.8000	1.98000
099.99	1	1	19.0001	1.90001
100.00	1	0	19.0000	1.90000
103.00	1	0	18.9700	1.89700
110.00	1	0	18.9000	1.89000
120.00	1	0	18.8000	1.88000
130.00	1	0	18.7000	1.87000
249.99	1	0	17.5001	1.75001
250.00	0	1	17.5000	1.75000
308.00	0	1	16.9200	1.69200

4.5.2.9.4 Bandswitch Switches Q4 and Q5

Bandswitch switches Q4 and Q5 limit the VCO frequency output to three bands in the Erect Mode (Table 4-6) and two bands in the Invert Mode (Table 4-7) with an approximate 1.4 MHz bandwidth. With a high input on BS1, pin 6 of connector P1, transistor Q4 conducts, adding inductor L2 in parallel to transformer T1. With transformer T1 and capacitor C16 providing the tank circuit for Q3, the adding of L2 in parallel to T1 reduces the inductance in the tank circuit, effectively shortens the transmission line from Q3, and increases the output frequency. The output from Q3 is applied to buffer amplifier Q6. The 16.032 MHz to 20.000 MHz output from Q6 is applied to LO input pin 8 of mixer U6 via an attenuator pad consisting of resistors R32, R33, and R34 and to the clock input pin 2 of divide-by-5/4 counter U4 via shaper Q7.

Table 4-7. Main Loop Assembly - Synthesizer Data (Invert Mode)

Demodulator Frequency (kHz)	Bandswitch Bits 1 0	Main Loop Frequency (MHz)	LO Frequency (MHz)
000.00	0 1	16.03200	2.00400
000.01	0 1	16.03208	2.00401
000.02	0 1	16.03216	2.00402
000.99	0 1	16.03992	2.00499
001.00	0 1	16.04000	2.00500
001.01	0 1	16.04008	2.00501
003.50	0 1	16.06000	2.00750
003.51	0 1	16.06008	2.00751
003.52	0 1	16.06016	2.00752
009.99	0 1	16.11192	2.01399
010.00	0 1	16.11200	2.01400
013.50	0 1	16.14000	2.01750
023.50	0 1	16.22000	2.02750
183.50	0 1	17.50000	2.18750
183.51	0 1	17.50008	2.18751
308.00	1 0	18.49600	2.31200

4.5.2.9.5 Mixer U6

The 22.10 MHz to 19.18 MHz (Erect Mode) or 18.16 MHz to 20.64 MHz (Invert Mode) output from pin 14 of coarse loop connector P2 is input to RF pin 1 of double-balanced mixer U6 via pin 3 of main loop connector P2. After being passed through the attenuator pad, the 16.032 MHz to 20.000 MHz output from Q6 is input to LO pin 8 of U6. The sum and difference of the two inputs are output from pins 3 and 4 through the low pass filter, composed of capacitors C32 through C35 and inductors L6, L8, and L9, amplifier Q8, and shaper Q9. This low pass filter passes only the difference frequency. This frequency is then input to VF pin 3 of phase detector U1.

4.5.2.9.6 Divide-By-Five/Four Counter U4

Counter U4, along with counter U5A described in paragraph 4.5.2.9.7, divide the VCO output by 10 (Erect Mode) or 8 (Invert Mode). Refer to Figure 4-25 for the following description.

With U/$\overline{D}$ input pin 1 tied low, counter U4 counts down, or divides, the input at clock input pin 2 by either 5 or 4. With a high input at pin 4 of connector P2 on the UPR/$\overline{INV}$ line from coarse loop NAND gate U2B and a low input at pin 5 of connector P2 on the INV/$\overline{UPR}$ line from coarse loop NAND gate U2A and input pin 6 of U4 tied low, the high input at pin 5 of U4 represents a decimal four. Counter U4 starts to count down from four on the first positive-going transition of the input at pin 2. It counts down to 0, at which time the output at pin 15 drops low for one count. On the next positive-going transition, U4 starts to count down from four. When the output at pin 15 dropped low, it caused counter U5A to change state.

4.5.2.9.7 Divide-By-Two Counter U5A

Counter U5A is a J-K flip-flop which changes state upon receipt of a negative-going transition at clock input pin 1. As a result, U5A changes state every 10 counts in the

Erect Mode and every eight counts in the Invert Mode. The output from U5A pins 5 and 6 fed through impedance matching transformer T3, attenuator pad R48, R49, R50, and low-pass filter C41, C43, and L7 to pin 13 of connector P2. The LO output signal is applied to pin 4 of connector P1 of Input Converter Assembly A1A4 described in paragraph 4.5.2.10.

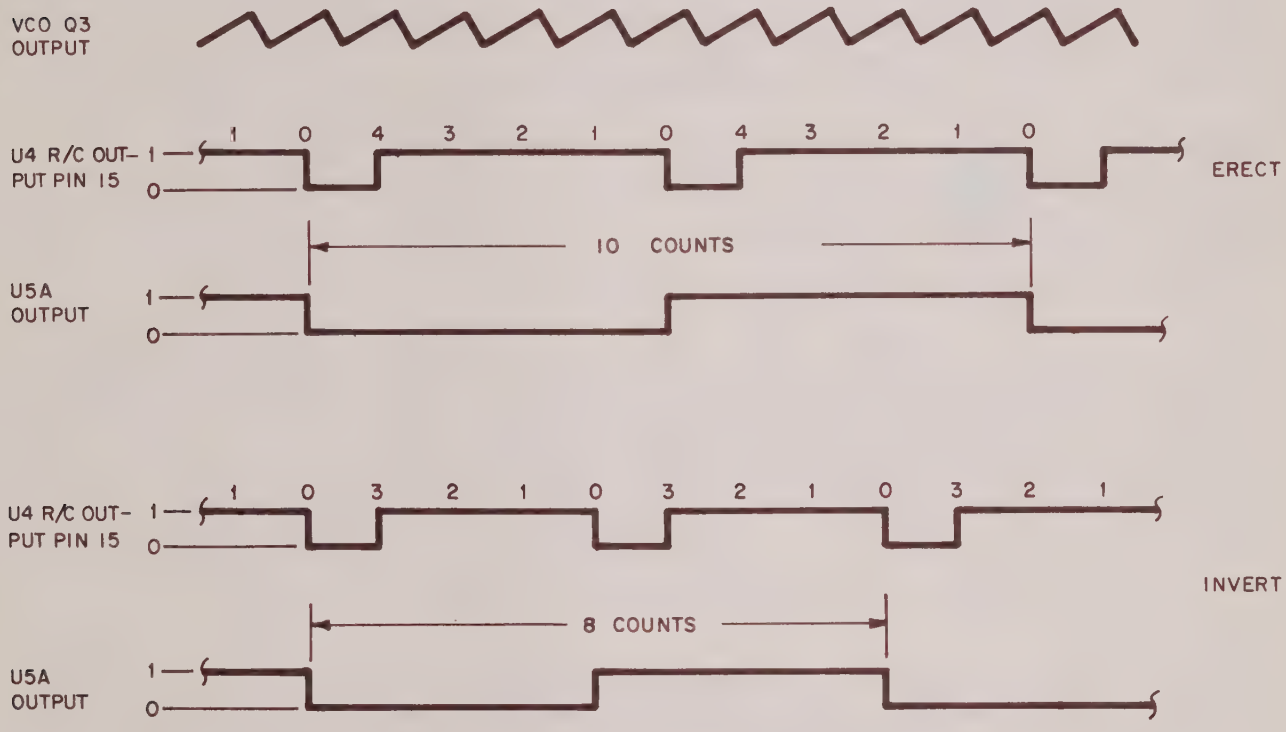

VCO Q3 OUTPUT
U4 R/C OUTPUT PIN 15
1 0 4 3 2 1 0 4 3 2 1 0
ERECT
10 COUNTS
U5A OUTPUT
U4 R/C OUTPUT PIN 15
1 0 3 2 1 0 3 2 1 0 3 2 1
INVERT
8 COUNTS
U5A OUTPUT

Figure 4-25. Divide-By-Ten/Eight Counters U4 and U5A Timing Diagram

4.5.2.10 Type 796071 Input Converter Assembly (A1A4)

Refer to Figure 4-26 for the functional block diagram and Figure 7-17 for the schematic diagram of Input Converter Assembly A1A4. Inputs to the input converter are the LO input signal, baseband input signal, and control signals for the contained attenuator pads.

In the erect mode, LO inputs from the main loop are from 2.000 MHz down to 1.692 MHz and in the invert mode, the LO inputs are from 2.004 MHz up to 2.312 MHz, as described in paragraph 4.5.2.9. The baseband input signals, from the baseband signal distribution amplifier described in paragraph 4.3.2, are from 200 Hz to 308 kHz. The attenuator pad control signals are either of two voltage levels, an approximate +15 Vdc to turn a pad on or an approximate -15 Vdc to turn a pad off. The attenuator pad control signals originate from the attenuator control assembly described in paragraph 4.5.2.11.

The outputs from the input converter are a 2 MHz signal and attenuator analog signals. The 2 MHz IF output is applied to the demodulator unit filter FL1. The analog signals are applied to the attenuator control assembly.

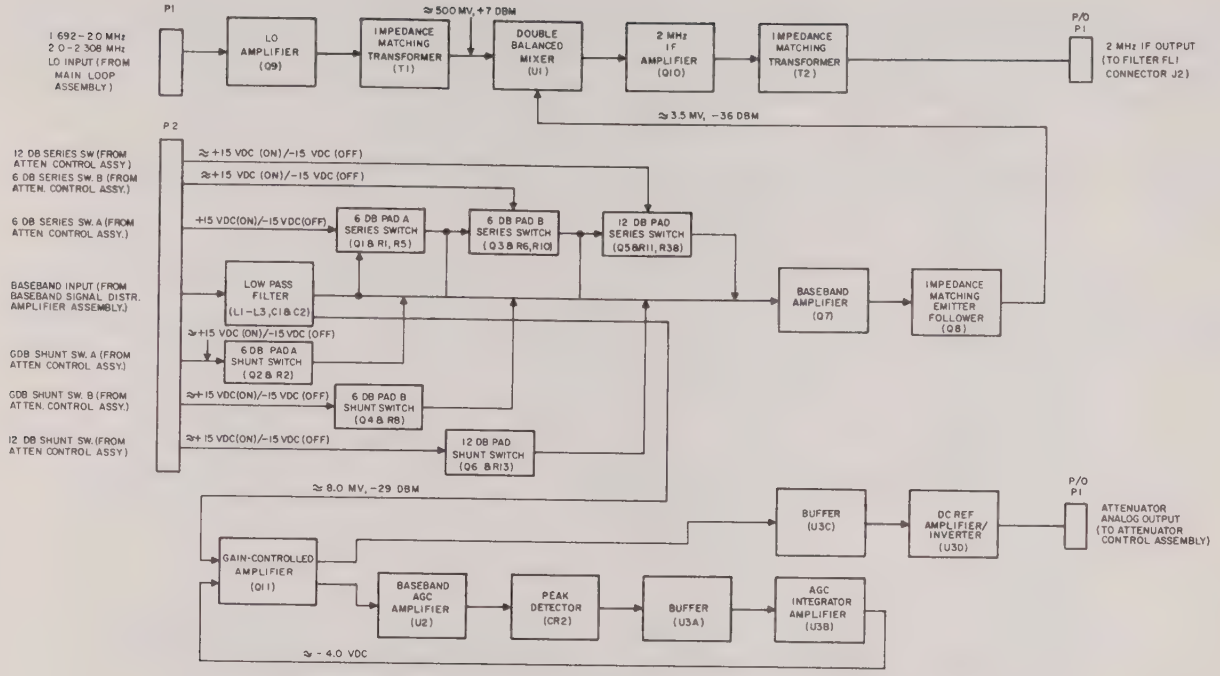

P1
1.692 - 2.0 MHz
2.0 - 2.308 MHz
LO INPUT (FROM MAIN LOOP ASSEMBLY)
LO AMPLIFIER (Q9)
≈500 MV, +7 DBM
IMPEDANCE MATCHING TRANSFORMER (T1)
DOUBLE BALANCED MIXER (U1)
2 MHz IF AMPLIFIER (Q10)
IMPEDANCE MATCHING TRANSFORMER (T2)
P/O P1
2 MHz IF OUTPUT (TO FILTER FL1 CONNECTOR J2)
≈3.5 MV, -36 DBM
P2
12 DB SERIES SW (FROM ATTEN CONTROL ASSY.)
6 DB SERIES SW. B (FROM ATTEN. CONTROL ASSY.)
6 DB SERIES SW. A (FROM ATTEN CONTROL ASSY.)
BASEBAND INPUT (FROM BASEBAND SIGNAL DISTR. AMPLIFIER ASSEMBLY)
6DB SHUNT SW. A (FROM ATTEN CONTROL ASSY.)
6DB SHUNT SW. B (FROM ATTEN. CONTROL ASSY.)
12 DB SHUNT SW. (FROM ATTEN CONTROL ASSY.)
≈+15 VDC (ON)/-15 VDC (OFF)
≈+15 VDC (ON)/-15 VDC (OFF)
+15 VDC(ON)/-15 VDC(OFF)
6 DB PAD A SERIES SWITCH (Q1 & R1, R5)
6 DB PAD B SERIES SWITCH (Q3 & R6, R10)
12 DB PAD SERIES SWITCH (Q5&R11, R38)
LOW PASS FILTER (L1-L3, C1 & C2)
BASEBAND AMPLIFIER (Q7)
IMPEDANCE MATCHING EMITTER FOLLOWER (Q8)
≈+15 VDC (ON)/-15 VDC (OFF)
6 DB PAD A SHUNT SWITCH (Q2 & R2)
≈+15 VDC(ON)/-15 VDC (OFF)
6 DB PAD B SHUNT SWITCH (Q4 & R8)
≈+15 VDC(ON)/-15 VDC (OFF)
12 DB PAD SHUNT SWITCH (Q6 &R13)
≈8.0 MV, -29 DBM
P/O P1
ATTENUATOR ANALOG OUTPUT (TO ATTENUATOR CONTROL ASSEMBLY)
BUFFER (U3C)
DC REF AMPLIFIER/ INVERTER (U3D)
GAIN-CONTROLLED AMPLIFIER (Q11)
BASEBAND AGC AMPLIFIER (U2)
PEAK DETECTOR (CR2)
BUFFER (U3A)
AGC INTEGRATOR AMPLIFIER (U3B)
≈ - 4.0 VDC

Figure 4-26. Input Converter Assembly Functional Block Diagram

The 2.000 MHz to 1.692 MHz (Erect Mode) or 2.004 MHz to 2.312 MHz (Invert Mode), after amplification by LO amplifier Q9, are applied to double-balanced mixer U1 where they are mixed with the baseband input signal. After being mixed by U1, the resultant 2 MHz output is amplified by 2 MHz IF amplifier Q10 and output to filter FL1. Filter FL1 removes the adjacent channels from the input. The 2.0002 MHz to 2.0034 MHz output from FL1 is applied to the IF demodulator assembly described in paragraph 4.5.2.12.

The analog output signals to the attenuator control assembly are converted into a 3-bit word which is used to determine which attenuator pads on the input converter will be placed in-line with the baseband input signals.

4.5.2.10.1 LO Amplifier Q9

The LO input at pin 4 of connector P1 is applied to LO amplifier Q9. Q9, with an amplification factor of 6, amplifies the input to a level of 1.35 mV. Resistor R27, in the collector circuit of Q9 provides proper impedance tranformation of the LO input through impedance matching transformer T1 to double-balanced mixer U1.

4.5.2.10.2 Double-Balanced Mixer U1

Double-balanced mixer U1 mixes the LO input at input L with the baseband input at input I. The sum and difference of the two inputs is output via output R through coupling capacitor C13 to 2 MHz IF amplifier Q10.

4.5.2.10.3 2 MHz IF Amplifier Q10

The IF output from U1 is amplified by a factor of 4.7 to a level of 9.3 mV. Variable resistor R37 provides an approximate 12 dB gain adjustment for the emitter of Q10. Resistor R34 in the output circuit of Q10 enables optimum reflected impedance through impedance matching transformer T2. Capacitor C15 resonates with the inductance of T2 at 2 MHz to provide additional gain in the IF output to input jack J2 of filter FL1.

4.5.2.10.4 Low-Pass Filter (L1 through L3, C1 and C2)

The 200 Hz to 308 kHz baseband input signals are input through pin 14 of connector P2 and filtered by a LC low-bandpass filter, comprised of inductors L1, L2, and L3, and capacitors C1 and C2. The filter has a 3 dB cutoff frequency of approximately 650 kHz. Capacitor C3, immediately following inductor L3, provides baseband signal coupling to gain controlled amplifier Q11.

4.5.2.10.5 Attenuator Pads

Baseband signal input attenuation is performed by three series attenuator pads and their associated parallel attenuator pads. The pads provide attenuation of the signal input in levels below the dynamic limits of amplifier Q7 and mixer U1 in levels from 0 dB to 24 dB in 6 dB steps. Each pad consists of two series resistors and their switch and a parallel resistor and its switch. For example, 6 dB pad A consists of series resistors R1 and R5, switch Q1, and parallel resistor R3 and switch Q2 as illustrated in Figure 4-27. The circuit switches when +15 Vdc is applied to FET Q2 and -15 Vdc is applied to Q1.

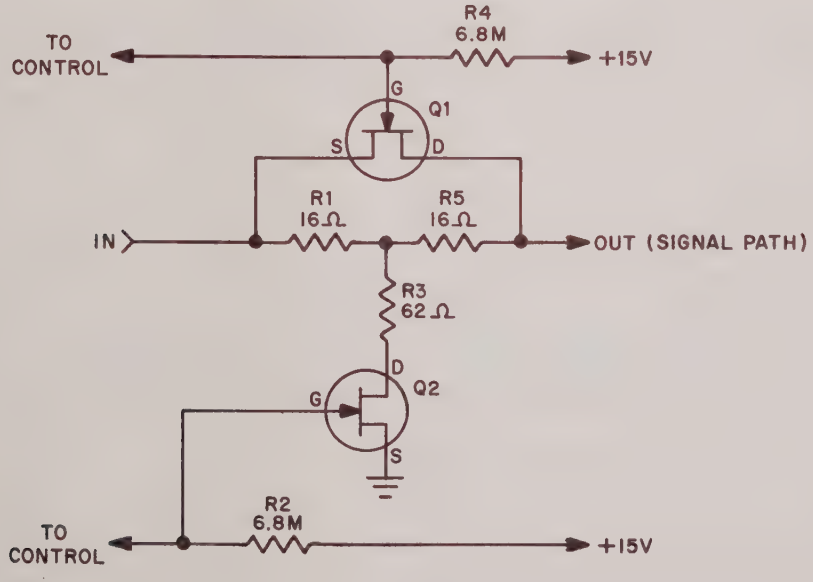


Figure 4-27. 6 dB Attenuator Pad A Circuit Diagram

The +15 Vdc and -15 Vdc control voltages are input to the input converter from the attenuator control assembly. The level of attenuation by the pads is determined by the input level of the baseband signal input as listed in Table 4-8. The level of the baseband signal input coupled through capacitor C3 to gain-controlled amplifier Q11 and output from pin 14 of connector P1 (ATTEN ANALOG OUTPUT) to the attenuator control determines the amount of attenuation placed on the input line.

Table 4-8. Input Level vs. Attenuator Pad State

Input Level (dBM)	Q1	Q2	Q3	Q4	Q5	Q6	Pad 6(A)	Pad 6(B)	Pad 12	Total Attenuation (dB)
-45 to -29	ON	OFF	ON	OFF	ON	OFF	OUT	OUT	OUT	0
-28 to -23	OFF	ON	ON	OFF	ON	OFF	IN	OUT	OUT	6
-22 to -17	OFF	ON	OFF	ON	ON	OFF	IN	IN	OUT	12
-16 to -11	ON	OFF	OFF	ON	OFF	ON	OUT	IN	IN	18
-10 to -5	OFF	ON	OFF	ON	OFF	ON	IN	IN	IN	24

The baseband signal input, after being attenuated as required by the 6 and 12 dB pads, is coupled through capacitor C4 to baseband amplifier Q7. The output from Q7 is applied to emitter follower Q8 which performs an impedance matching function of the baseband input to double-balanced mixer U1.

4.5.2.10.6 Gain-Controlled Amplifier Q11

The baseband signal, via capacitor C3 described in paragraph 4.5.2.10.4, is input to pin 3 of gain-controlled amplifier Q11. Amplifier Q11 provides the analog voltage, coincident with the baseband input level, to the attenuator control which, in turn, switches the attenuator pads described in paragraph 4.5.2.10.5. The output from pin 1 of Q11 is applied to baseband AGC amplifier U2.

4.5.2.10.7 Baseband AGC Amplifier U2

Baseband amplifier U2 further amplifies the baseband input signal to drive peak detector CR2. Resistor R58 sets U2 gain to times 66. Resistor R60 reduces the transient response of the peak detector circuit consisting of diode CR2, capacitor C22, and resistor R61. The output from the peak detector is applied to buffer U3A which isolates AGC integrator amplifier U3B. The approximately -4.0 Vdc output from U3B is applied to buffer U3C and then, in turn, through DC reference amplifier/inverter U3D to the attenuator control assembly.

4.5.2.11 Type 796066 Attenuator Control Assembly (A1A5)

Refer to Figure 4-28 for the functional block diagram and Figure 7-18 for the schematic diagram of Attenuator Control Assembly A1A5. The attenuator control assembly contains the attenuator control circuit and the audio switch circuit. The attenuator control circuit converts the attenuator analog input from the input converter, described in paragraph 4.5.2.10, into control signals for the attenuator pad switches described in paragraph 4.5.2.10.5. The audio switch circuit enables selection of an audio output through the phones jack on the front panel of the control unit.

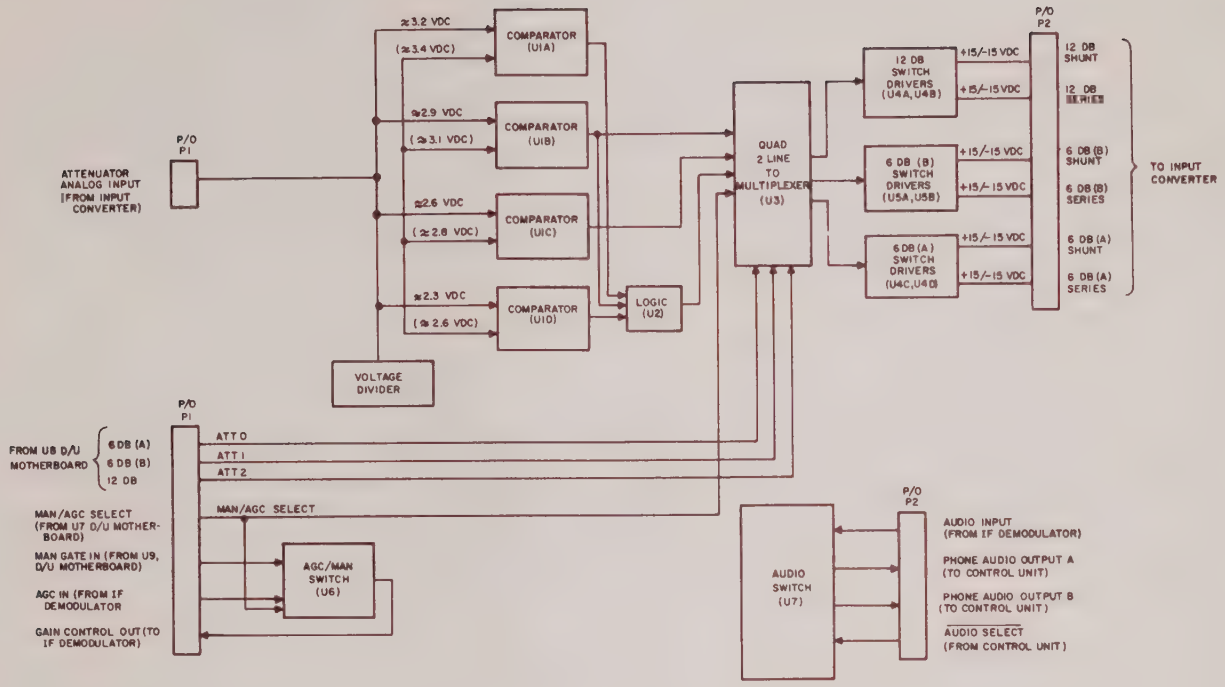


Figure 4-28. Attenuator Control Assembly Functional Block Diagram

4.5.2.11.1 Comparator U1

The attenuator analog input from the input converter is applied to comparator U1 which compares the voltage level of the input against established reference voltages from the voltage divider network. When the baseband input signal to the input converter are below AGC threshold (-29 dBm), the analog input to U1 is less than the established reference voltages and the outputs from U1A through U1D are all low. When the attenuator input voltage levels exceed the input voltages listed in Table 4-9, U1A through U1D switch to the states indicated. The outputs from U1A, U1B, and U1D are applied to logic U2 which enables the four outputs from comparator U1 to be converted into three inputs to quad 2-line-to-1-line multiplexer U3.

Table 4-9. U1A through U1D State - Input Voltage

Input Voltage (±50 MV)	State			
	U1D	U1C	U1B	U1A
2.38	L	L	L	L
2.38	H	L	L	L
2.65	H	H	L	L
2.95	H	H	H	L
3.18	H	H	H	H

4.5.2.11.2 Quad 2-Line-to-1-Line Multiplexer (U3)

Multiplexer U3 enables switching of attenuation level coding in either the manual or AGC mode of operation. With a high input to pin 13 of connector P1 from motherboard driver U7, described in paragraph 4.5.2.3, the level at pin 1 of U3 is high. When pin 1 of U3 is high, the data (ATT0, ATT1, ATT2) at input pins 3, 6, and 10 is output from U3 at pins 4, 7, and 9 to switch drivers U4 and U5. When the level at pin 1 is low, AGC mode of operation, the data at input pins 2, 3, and 11 is output at pins 4, 7, and 9 to the switch drivers. Table 4-10 provides the U3 output levels for the 5 attenuation levels.

4.5.2.11.3 Switch Drivers U4A through U4D, U5A and U5B

Switch drivers U4A through U4D, U5A, and U5B provide the paired +15 Vdc and -15 Vdc outputs to the attenuator pads described in paragraph 4.5.2.10.5. For example, assuming a high output at pin 4 of U3 and low outputs at pins 7 and 9 (refer to Table 4-10, 6 dB attenuation), the input to pin 9 of U4C is high and the input to pin 11 of U4D is high. The high input at pin 9 of U4C results in a +15 Vdc output via pin 5 of connector P2 (6 dB-A SHUNT) to input converter switch Q2 placing shunt resistor R3 on line. The high input at pin 11 of U4D results in a -15 Vdc output via pin 6 of connector P2 (6 dB-A SERIES) to input converter switch Q1 placing series resistors R1 and R5 on the baseband input line.

Table 4-10. Multiplexer U3 Outputs - Attenuation Levels

Attenuation	Outputs								Outputs		
(dB)	U1D	U1C	U1B	U1A	U2D	U2C	U2B	U2A	U3 1Y (Pin 4)	U3 2Y (Pin 7)	U3 3Y (Pin 9)
0	L	L	L	L	L	L	L	H	L	L	L
6	H	L	L	L	H	L	L	L	H	L	L
12	H	H	L	L	H	L	L	L	H	H	L
18	H	H	H	L	L	L	H	L	L	H	H
24	H	H	H	H	H	L	L	L	H	H	H

4.5.2.11.4 Audio Switch U7

Audio switch U7, Figure 4-29, passes the audio output signal from the IF demodulator to the control unit phones jack upon receipt of a low at pin 8 of connector P2 (AUDIO SELECT). It is a quad transistor package with Q2 and Q3 configured as a differential amplifier. Transistors Q2 and Q3 are biased from the -15 Vdc supply to provide approximately 0 Vdc at their collectors. Transistors Q1 and Q4 provide the switching function for U7 via the input at pin 8 of connector P2 (AUDIO SELECT). A low input at pin 8 is of insufficient amplitude to turn Q1 and Q4 on with Q2 and Q3 already conducting. A high input at pin 8 biases Q1 and Q4 on, providing a low impedance to ground through the capacitor and a high impedance to the output via the now turned-off transistors Q2 and Q3.

4.5.2.11.5 AGC/MAN Switch U6

AGC/MAN switch U6 provides the capability of switching either the manual gain input from motherboard digital-to-analog converter U9, described in paragraph 4.5.2.6, or the AGC input from AGC integrator U2B on the IF demodulator assembly, described in paragraph 4.5.2.12, to the gain control output line to gain-controlled amplifier Q1 on the IF demodulator assembly.

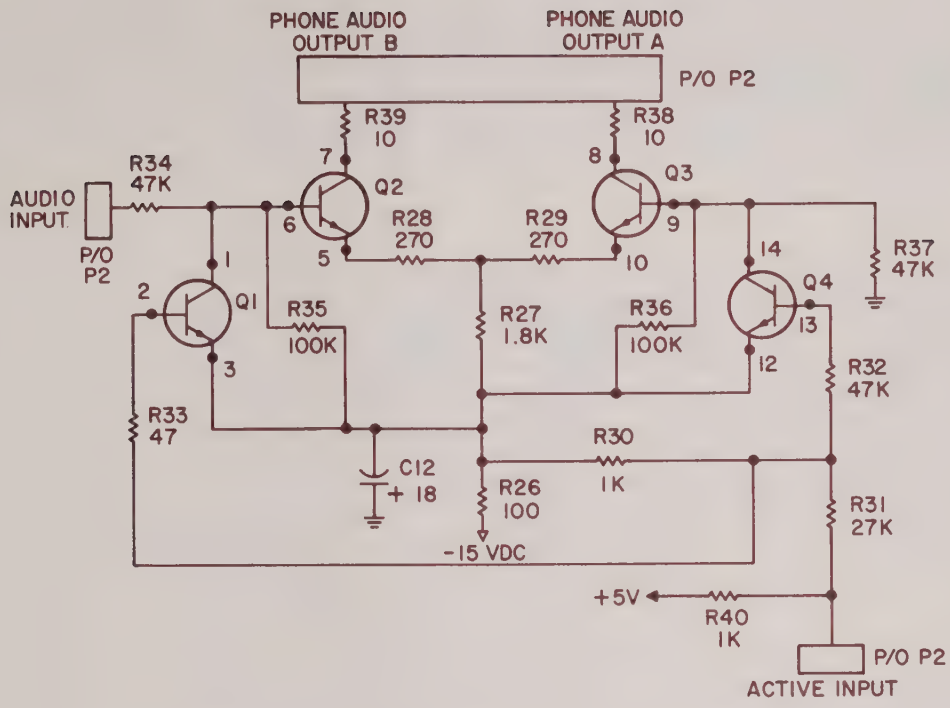


Figure 4-29. Audio Switch U7 Circuit Diagram

A high input to pin 3 of U6 via pin 13 of connector P1 (MAN/$\overline{\text{AGC}}$) from motherboard driver U7 causes the input at pin 2 to be fed to pin 6. This allows the manual gain input at pin 4 of connector P1 (MAN GAIN IN) to be passed through U6 to output pin 8 of connector P1.

A low input to pin 3 of U6 causes the input at pin 9 to be fed to pin 10 and opens the path between pins 2 and 6. This allows the AGC input at pin 6 of connector P1 (AGC IN) to be passed through U6 to output pin 8.

4.5.2.12 Type 796069 IF Demodulator Assembly (A1A6)

Refer to Figure 4-30 for the functional block diagram and Figure 7-19 for the schematic diagram of IF Demodulator Assembly A1A6. The IF demodulator mixes the 2.0002 MHz to 2.0034 MHz input from filter FL1 with the 2.0 MHz reference input signal from the reference generator assembly, described in paragraph 4.3.6, via 2 MHz reference buffer, described in paragraph 4.5.2.5. The resultant 200 Hz to 3400 Hz audio signal is supplied to the control unit phones jack via attenuator control audio switch U7, described in paragraph 4.5.2.11.4, and to control rack frame audio output connector J3. The IF demodulator also provides the AGC input to AGC/MAN switch U6, described in paragraph 4.5.2.11.5.

4.5.2.12.1 Gain-Controlled Amplifier Q1

The 2.0002 MHz to 2.0034 MHz IF input from filter FL1 is applied to pin 3 of gain-controlled amplifier Q1. Amplifier Q1 is a dual-gate FET which provides gain-controlled amplification of the IF signal. The gain control input to Q1 via pin 8 of connector P1 from

AGC/MAN switch U6 originates from two circuits, as described in paragraph 4.5.2.11.5. The gain of Q1 is a nominal 27 dB. Adjustable resistor R11 provides variable degeneration in the source by-pass which enables the gain of Q1 to be varied ±3 dB from the nominal. Inductor L1 prevents degenerative feedback. The 40 mV output from pin 1 of Q1 is coupled through capacitor C31 to pin 1 of the product detector U1 and is applied to AGC IF amplifier Q4.

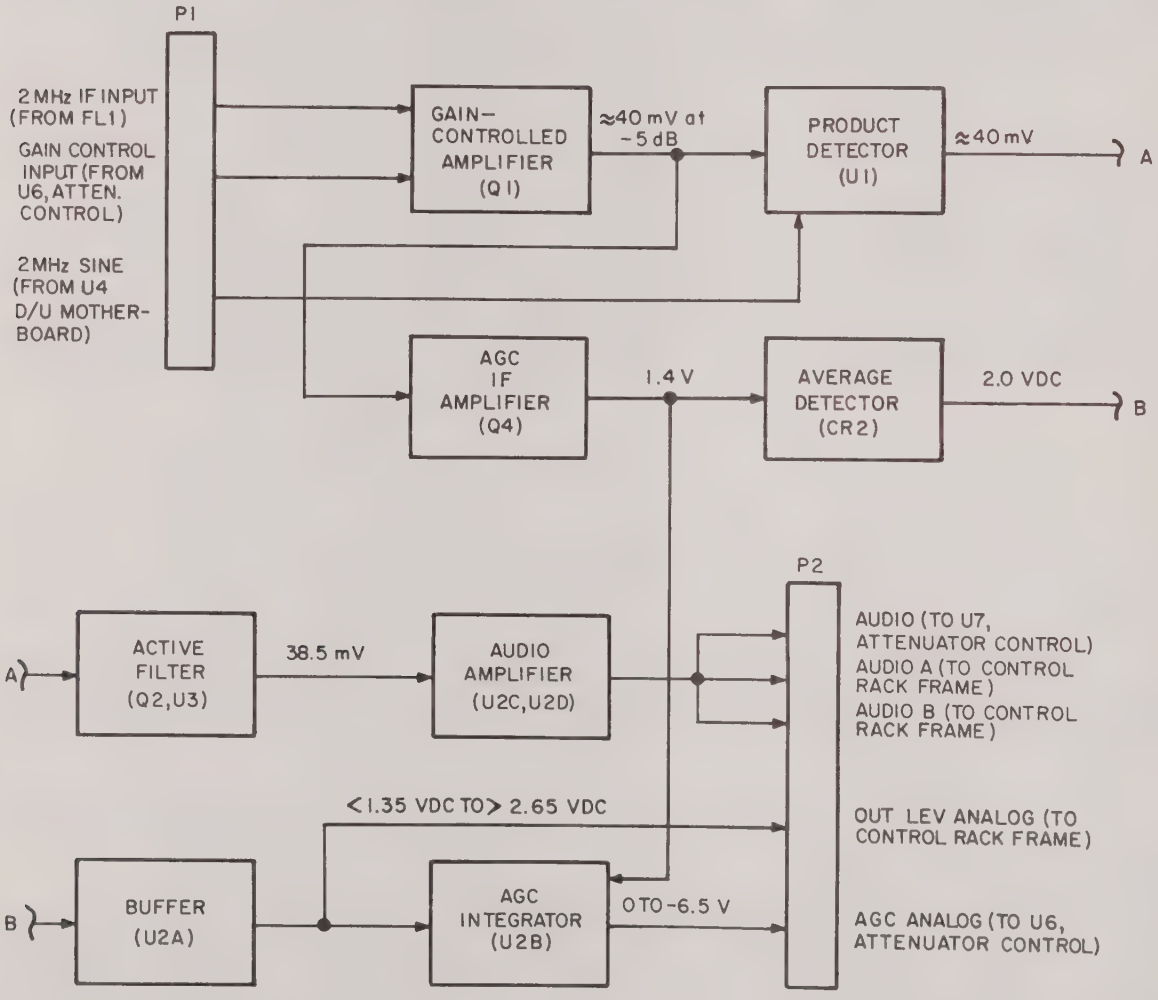


Figure 4-30. IF Demodulator Functional Block Diagram

4.5.2.12.2 Product Detector U1

The 40 mV output from Q1 is input to product detector U1 where it is mixed with the 2.0 MHz reference input from the 2 MHz reference generator via 2 MHz reference buffer U4 on the motherboard. Potentiometer R16 provides the means to null carrier feedthrough. Resistor R20 establishes a 0.5 ma bias current for U1 and R15 restores maximum input signal handling which is a product of bias current and the value of R15. The 40 mV output from U1 is applied to active filter Q2 and U3, which removes 3rd LO feedthrough and rejects image frequencies. The resultant audio signal is fed to audio amplifiers U2C and U2D.

4.5.2.12.3 Audio Amplifiers U2C and U2D

Amplifiers U2C and U2D amplify the audio input by a factor of 26.5. Resistors R36 and R57, associated with U2C and U2D, respectively, provide impedance matching for the audio output on the rear panel of the control rack frame. The audio output at pin 11 of connector P2 is fed to audio switch U7 on the attenuator control described in paragraph 4.5.2.11.4.

4.5.2.12.4 AGC IF Amplifier Q4

AGC IF amplifier Q4 is a dual gate FET which amplifies the 40.0 mV audio output from gain-controlled amplifier Q1. It provides a high input impedance and low capacitive feedback for maximum isolation of average detector CR2 from the signal path. A common resistance divider (R37, R38, and R39) provides gate biasing while variable resistor R45 provides the necessary gain control to set AGC threshold. Resistor R42, in the drain circuit, suppresses spurious oscillations while inductors L2 and L3 resonate with the output, stray capacitance, and capacitor C24 at approximately 2.0 MHz. Resistor R40 sets the 3 dB bandwidth to approximately 400 kHz. At AGC threshold, the signal level applied to average detector CR2 is approximately 160 mV rms.

4.5.2.12.5 Average Detector CR2

Average detector CR2, a Schottky Diode, is used for its low turn-on voltage. It is forward biased to raise the detector anode voltage to improve low-level sensitivity and linearity. Capacitor C26 and resistor R47 provide peak detection of the 2.0 MHz IF while allowing the average response of the detector to be in the 200 Hz to 3400 Hz range.

4.5.2.12.6 Buffer U2A

Buffer U2A provides a high impedance load for average detector CR2. This reduces the intermodulation products resulting from the lower power requirements of CR2. The analog output from U2A, from 1.35 Vdc to 2.65 Vdc, is applied to the output level and to AGC integrator U2B.

4.5.2.12.7 AGC Integrator U2B

The non-inverting input of AGC Integrator U2B is set to approximately +2 V to provide AGC delay or threshold to occur at approximately -5 dBm of the signal level output. Capacitor C29 charges through resistor R51 to the positive going output of U2A. The output is within a nominal 3 dB 45 msec after a 40 dB input increase. Capacitor C29 discharges through a larger impedance providing slow AGC decay. Resistor R53 limits dc gain while R54 is damping to prevent overshoot. The AGC output is fed to attenuator AGC/MAN select switch U6 on Attenuator Control.

4.5.3 TYPE 796067 DISPLAY BOARD ASSEMBLY (A2) AND TYPE 796068 DISPLAY DRIVER ASSEMBLY (A3)

Refer to Figure 7-20 for the schematic diagram of Display Board Assembly A2. The 8-bit shift and storage registers U1 and U2 of the display driver, refer to Figure 4-31 for the functional block diagram and Figure 7-21 for the schematic diagram, receive and decode the frequency display word of the data input from the control unit microprocessor. The decoded data is then input to display drivers U3 through U7 which, in turn, are used to drive the frequency display on Display Board Assembly A2.

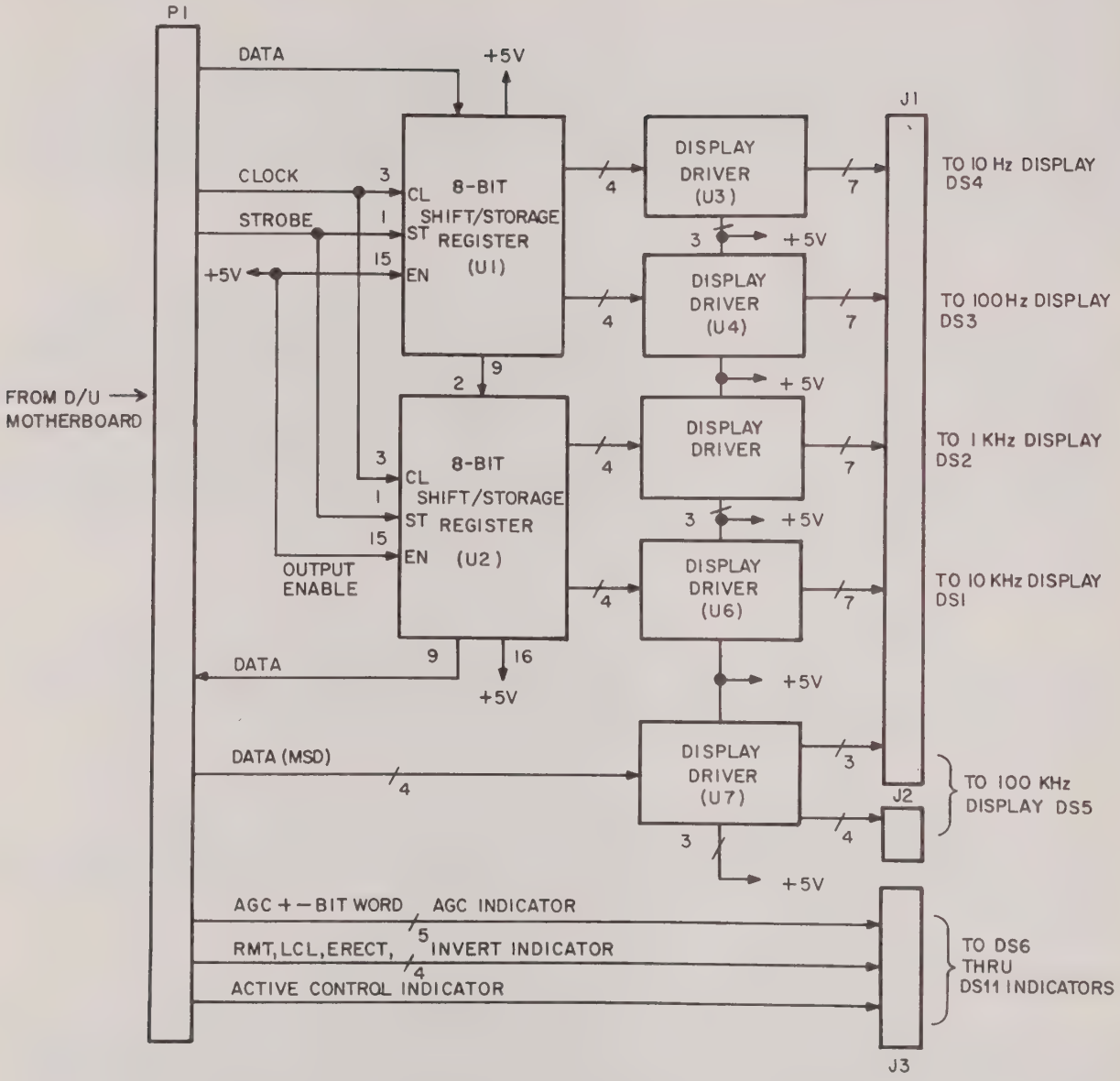


Figure 4-31. Display Driver Functional Block Diagram

4.5.3.1 8-Bit Shift/Storage Registers U1 and U2

Shift/Storage registers U1 and U2, along with shift/storage registers U10, U11, U12, U8, and U6, described in paragraph 4.5.2.2, form the demodulator unit control register. They control the four least significant digits of the frequency display, DS4, DS3, DS2, and DS1. The MSD control bits, D3 through D0, are decoded by shift/storage register U6 and input to display driver U7 described in paragraph 4.5.3.2.

Serial data containing the 4 LSD bits of the frequency display word are input to pin 2 of register U1 via pin 13 of connector P1. With the output enable pin, pin 15, of U1 and U2 tied high to +5 Vdc via pin 12 of connector J3, a positive-going strobe pulse at input pin 1

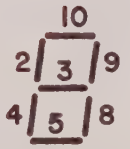
transfers data in U1 and U2 through their respective storage registers to their output pins 7, 6, 5, 4, 11, 12, 13, and 14. The data at the output pins is applied to input pins 7, 1, 2, and 6 of display drivers U3, U4, U5, and U6. The MSD bits of the frequency display word are transferred from motherboard register U6 to display driver U7 upon receipt of the same positive-going strobe pulse.

4.5.3.2 Display Drivers U3 through U7

Refer to Table 4-11 for the following description. Display drivers U3 through U7 are standard BCD-to-seven-segment decoders/drivers. With pins 3, 4, and 5 tied high to +5 Vdc via pin 12 of connector J3, BCD data at input pins 7, 1, 2, and 6 are decoded and output at pins 13, 12, 11, 10, 9, 15, and 14 (a, b, c, d, e, f, and g respectively) as a low (ground) or high (4 Vdc) to the segment inputs of displays DS1 through DS5. With pins 1 and 6 of the displays tied high to +4 Vdc, a low input to a segment circuit causes the segment to light.

Table 4-11. Display Driver to Display Relationships

Decimal	Inputs to U3 Through U7				Outputs from U3 Through U7/Inputs to DS1 Through DS5						
	Pin 6	Pin 2	Pin 1	Pin 7	Pin 13/10	Pin 12/9	Pin 11/8	Pin 10/5	Pin 9/4	Pin 15/2	Pin 14/3
0	L	L	L	L	L	L	L	L	L	L	H
1	L	L	L	H	H	L	L	H	H	H	H
2	L	L	H	L	L	L	H	L	L	H	L
3	L	L	H	H	L	L	L	L	H	H	L
4	L	H	L	L	H	L	L	H	H	L	L
5	L	H	L	H	L	H	L	L	H	L	L
6	L	H	H	L	H	H	L	L	L	L	L
7	L	H	H	H	L	L	L	H	H	H	H
8	H	L	L	L	L	L	L	L	L	L	L
9	H	L	L	H	L	L	L	H	H	L	L



DS1 through DS5 Segment Identification

4.5.3.3 Type 796067 Display Board Assembly (A2)

Refer to Figure 4-32 for the functional block diagram and Figure 7-20 for the schematic diagram of Display Board Assembly A2. The decoded data from display drivers U3 through U7, described in paragraph 4.5.3.2, is input to and displayed by displays DS1 through DS5. Gain data in BCD format is input to BCD-to-decimal decoder/driver U1 from the control unit via motherboard A1, described in paragraph 4.5.2, and display driver A2. REMOTE, LOCAL, INVERT, ERECT, AGC ON, and ACTIVE CONTROL data, from register U6 and driver U7 on the motherboard, is displayed by indicators DS6, DS7, DS8, DS9, DS10, and one indicator of DS11 upon receipt of a low input at pins 3, 4, 5, 6, 11, and 12 of connector P3.

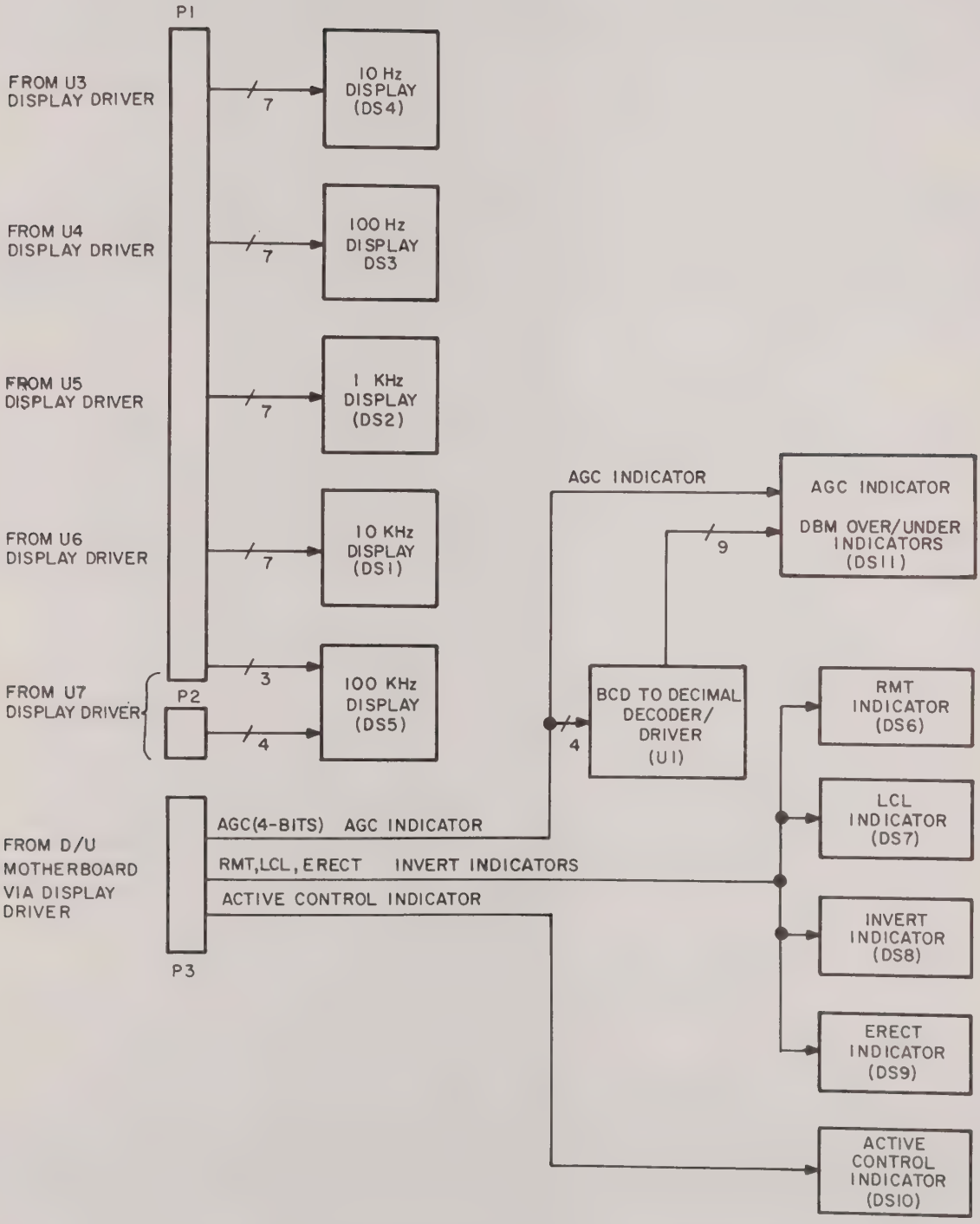


Figure 4-32. Display Board Functional Block Diagram

4.5.3.3.1 Displays DS1 Through DS5

Data stream frequency data decoded by display drivers U3 through U7 is input to displays DS1 through DS5 via their input pins listed in Table 4-11. With pin 1 and 6 of the displays tied high to +4 Vdc, a low input to a listed input pin causes the associated segment to light.

4.5.3.3.2 BCD-To-Decimal Decoder/Driver U1

Refer to Table 4-12 for the following description. Gain data in BCD format, from the control unit via the motherboard and display driver assembly A2 are input to BCD-to-Decimal decoder/driver U1 where the data are decoded for display by DS11. With the DS11 indicators tied high to +4 Vdc, a low input to an indicator causes the indicator to light. The LEV 3 through LEV 0 gain data is input to U1 pins 12 through 15 via pins 7, 6, 5, and 4 of connector P3.

Table 4-12. Decoder/Driver U1 Inputs/Outputs to DS11 Relationships

Inputs				Outputs									DS 11
Pin 12	Pin 13	Pin 14	Pin 15	Pin 9	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 10	Indicator ON
L	H	H	H	L	H	H	H	H	H	H	H	H	Over
L	H	H	L	H	L	H	H	H	H	H	H	H	-2
L	H	L	H	H	H	L	H	H	H	H	H	H	-3
L	H	L	L	H	H	H	L	H	H	H	H	H	-4
L	L	H	H	H	H	H	H	L	H	H	H	H	-5
L	L	H	L	H	H	H	H	H	L	H	H	H	-6
L	L	L	H	H	H	H	H	H	H	L	H	H	-7
L	L	L	L	H	H	H	H	H	H	H	L	H	-8
H	L	L	L	H	H	H	H	H	H	H	H	L	Under

(This page intentionally left blank.)

SECTION V

MAINTENANCE

5.1 GENERAL

This section contains preventive and corrective maintenance procedures for the Demodulator.

5.2 PREVENTIVE MAINTENANCE

The Demodulator has been designed for optimum performance over extended periods of time with minimal maintenance. However, cleaning, visual inspections, and performance tests should be accomplished at regular intervals. Table 5-1 lists the recommended time intervals for the various preventive maintenance procedures and adjustments.

Table 5-1. Preventive Maintenance Procedure and Adjustment Schedules

Procedure/Adjustment	Recommended Interval	Comments
Cleaning (Para. 5.2.1.1)	60 Days	Interval variable dependent upon operating environment.
Lubrication (Para. 5.2.1.2)	-	No lubrication required.
Visual Inspection (Para. 5.2.2)	60 Days	Interval variable dependent upon operating environment and equipment use.
Performance Tests (Para. 5.2.3)	180 Days	Interval variable dependent upon operating environment and equipment use.
Adjustment Procedures	-	No mechanical adjustments. No anticipated electrical adjustment/alignment.

5.2.1 CLEANING AND LUBRICATION

5.2.1.1 Cleaning

The Demodulator should be kept free of dust, moisture, grease, and other foreign matter to ensure trouble-free operation. Use low pressure compressed air, if available, to remove accumulated dust from the interior and exterior surfaces of the unit. A clean, dry, lint-free cloth or a soft bristled brush, as a camera lens brush, may also be used. A clean, lint-free cloth moistened with 1, 1, 1-trichloroethane (methyl chloroform), or equivalent, may be used on interior and exterior surfaces (see WARNING PAGE at front of this document for personnel hazards involving use of 1, 1, 1-trichloroethane).

5.2.1.2 Lubrication

The Demodulator does not require lubrication of any mechanical assemblies. However, when replacing any transistors which have heat radiators or are mounted on the chassis and use silicon grease to aid in heat transfer, be sure to replace the silicon grease also.

5.2.2 INSPECTION

Many potential or existing troubles can be detected by making a visual inspection of the Demodulator. For this reason, a complete visual inspection should be performed at a regular interval.

Inspect for components showing signs of deterioration. If discovered, check components and associated circuitry to verify proper operation. Damage caused by overheating may be the result of other less apparent troubles in the circuit. The cause of overheating should be determined and corrected prior to replacing any damaged parts.

Inspect pin connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

When accessible, inspect printed circuit boards for damaged tracks (conductors), loose connections, corrosion, or other signs of deterioration. If damaged tracks are discovered, repair using procedures in paragraph 5.3.5.5. If corrosion is discovered on printed circuit boards, clean using procedures in paragraph 5.3.5.5.

5.2.3 PERFORMANCE TEST PROCEDURES

5.2.3.1 Introduction

The procedures outlined in this paragraph are prepared for use by maintenance technicians to verify Demodulator compliance with specifications or to generate specific fault symptoms for troubleshooting. Demodulators being returned to service after repair should be tested using these procedures to verify proper operation.

5.2.3.2 Performance Standards

Table 5-2 summarizes the various electrical parameters tested in this paragraph. To be acceptable for service, demodulators should meet or exceed all standards listed.

Table 5-2. Demodulator Performance Standards

Parameter	Performance Standard
1. Function of Controls/Indicators	Must function per paragraph 3.2.2.
2. Baseband Freq. Response and Output Level	±1 dB from 200 Hz to 308 kHz.
3. Baseband - VF conversion Gain	40 dB at 000.00 kHz, 111.11 kHz, 222.22 kHz, 244.44 kHz, 288.88 kHz, and 308.00 kHz.
4. Headphone Output Capability	+10 dBm minimum for 1.71 mV B-B input.
5. Tuning Accuracy	±5 Hz at 000.00, 222.22 and 308.00 kHz.
6. AGC Range	3 dB (maximum) output change for input change from -45 dBm to -5 dBm.

Table 5-2. Demodulator Performance Standards (Continued)

Parameter	Performance Standard
7. Manual Gain Control Range	40 dB (minimum)
8. Residual Noise	-65 dBm at audio output at 100 kHz.
9. Demodulator Crosstalk	60 dB attenuation between demodulators on the same chassis.
10. Adjacent Channel Rejection	45 dB at 3800 Hz ±200 Hz.

NOTE

The above parameters relate only to the Baseband-to-VF Demodulation capability in local mode. Performance of remote and data output functions must be verified with suitable peripheral terminals.

5.2.3.3 General Guidelines

When performing the test procedures, the maintenance technician should comply with the following instructions:

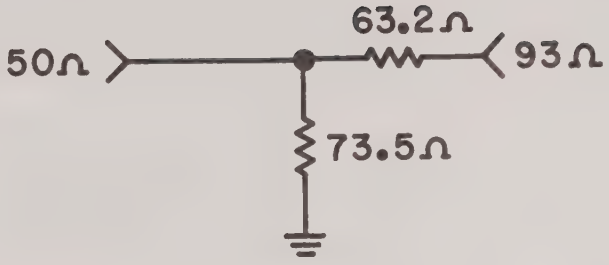
1. Read each paragraph carefully from beginning to end before attempting to perform the test described in the paragraph.

2. Allow a minimum of 30 minutes warm-up time for the test equipment prior to performing any of the tests.

3. Hook up the test equipment as indicated in the appropriate figure for the test. Alternate test equipment which performs the same function as equipment illustrated and listed below may be used unless otherwise noted.

   HP 3330B Signal Synthesizer (or equivalent)
   HP 3400A TRMS Voltmeter (or equivalent)
   HP 334, 334A, or 334B Distortion Analyzer (or equivalent)
   HP 1202A Oscilloscope (or equivalent)
   HP 5383 Frequency Counter (or equivalent)
   50 Ω-to-93 Ω Minimum Loss Pad (fabricated locally as shown on the next page)
   600 Ω Resistor

4. Perform the tests in the order given. If any specified result is not obtained, refer to paragraph 5.3 for fault isolation and correction.



5.2.3.4 Controls/Indicators Performance Tests

1. Set Demodulator front panel controls as follows:

a.	POWER	- Off
b.	DEMODULATOR SELECT	- 1
c.	Phones LEVEL	- Max. CCW
d.	STEP SIZE HZ	- 10
e.	STEP RATE/SEC	- 1

2. Set rear panel voltage select switch S2 to match available ac line voltage.

3. Set Demodulator POWER switch to ON position. The POWER ON indicator lights and all demodulator unit frequency displays light (disregard displayed numerals).

4. Verify that selected demodulator unit ACTIVE control indicator and LCL indicator are both lit.

5. Depress the ERECT/INVERT button several times. The ERECT and INVERT indicators light alternately.

6. Depress the MAN/AGC button several times. The AGC indicator alternately lights and goes out.

7. Switch the TUNE switch between UP and DOWN positions. The 10 Hz frequency display digit increments and decrements at a rate of 1 digit per second between 000.00 and 308.00 limits.

8. Set STEP SIZE HZ switch to 100 and switch the TUNE switch between UP and DOWN positions. The 100 Hz frequency display digit increments and decrements at a rate of 1 digit per second between 000.00 and 308.00 limits.

9. Set STEP SIZE HZ switch to 1 k and switch the TUNE switch between UP and DOWN positions. The 1 kHz frequency display digit increments and decrements at a rate of 1 digit per second between 000.00 and 308.00 limits.

10. Set STEP RATE/SEC switch to 10 and switch the TUNE switch between UP and DOWN positions. The 1 kHz frequency display digit increments and decrements at a rate of 10 digits per second between 000.00 and 308.00 limits.

11. Set STEP RATE/SEC switch to 100 and switch the TUNE switch between UP and DOWN positions. The 1 kHz frequency display digit increments and decrements at a rate of 100 digits per second between 000.000 and 308.00 limits.

12. Tune demodulator unit to 000.00 kHz, as indicated on frequency display.

13. Repeat steps 4 through 12 for demodulator units 2, 3 and 4 using the DEMODULATOR SELECT switch to select each demodulator unit.

14. Set Demodulator POWER switch of off position.

5.2.3.5 Baseband Frequency Response Test

1. Connect test equipment to the Demodulator as shown in Figure 5-1.

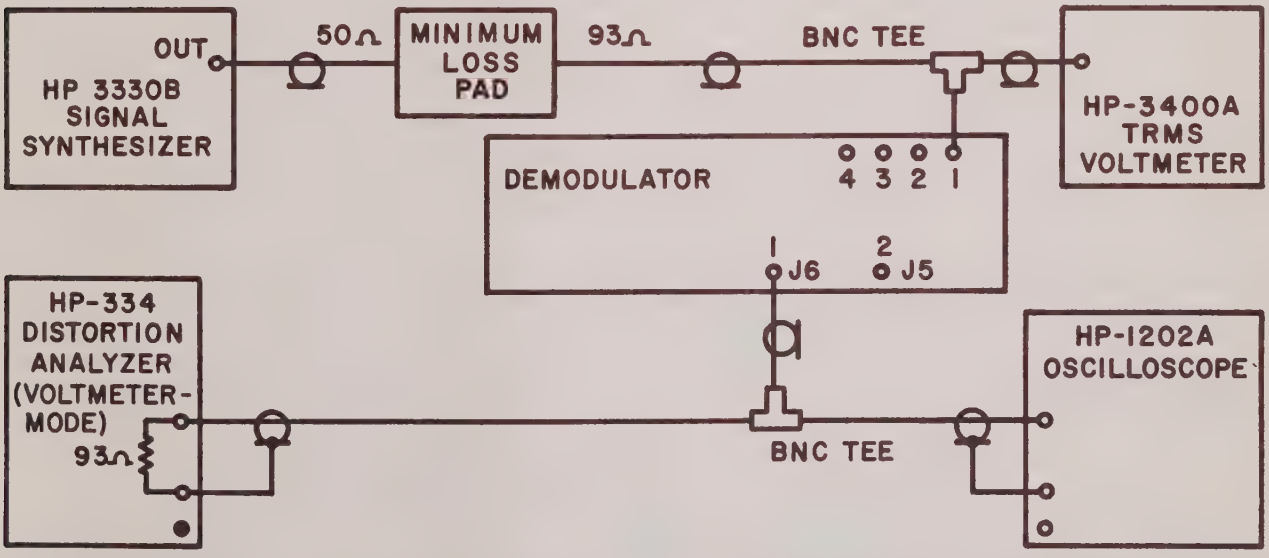


Figure 5-1. Test Setup, Baseband Frequency Response and Output Level Test

2. Set signal synthesizer output frequency to 200 Hz and output level to 1.0 V rms as indicated on TRMS voltmeter.

3. Set rear panel switches S1, S2, and S3 to BRDG positions.

4. Set Demodulator POWER switch to ON position and measure baseband output level. The output level is 1.0 V rms, ±1 dB, as

indicated on distortion analyzer (voltmeter mode). The oscilloscope displays a sinusoidal waveform.

5. While observing distortion analyzer (voltmeter mode) for variation, slowly increase signal synthesizer output frequency to 308 kHz. Variation is less than 0.5 dB.

6. Disconnect measuring lead from connector J6 and connect to connector J5.

7. Measure baseband output level. Baseband output is 1.0 V rms, ±1 dB. The oscilloscope displays a sinusoidal waveform.

8. While observing distortion analyzer (voltmeter mode) for variation, slowly decrease signal synthesizer output frequency to 200 Hz. Variation is less than 0.5 dB.

9. Set rear panel switch S1 to INDEP position, connect input test lead to input connector 2, and repeat step 5.

10. Disconnect measuring lead from connector J5 and connect to connector J6.

11. Set rear panel switch S2 to INDEP position, connect input test lead to input connector 3, and repeat step 8.

12. Set rear panel switch S3 to INDEP position, connect input test lead to input connector 4, and repeat step 5.

5.2.3.6 Baseband - Video Frequency (VF) Conversion Test

1. Connect test equipment to Demodulator as shown in Figure 5-2.

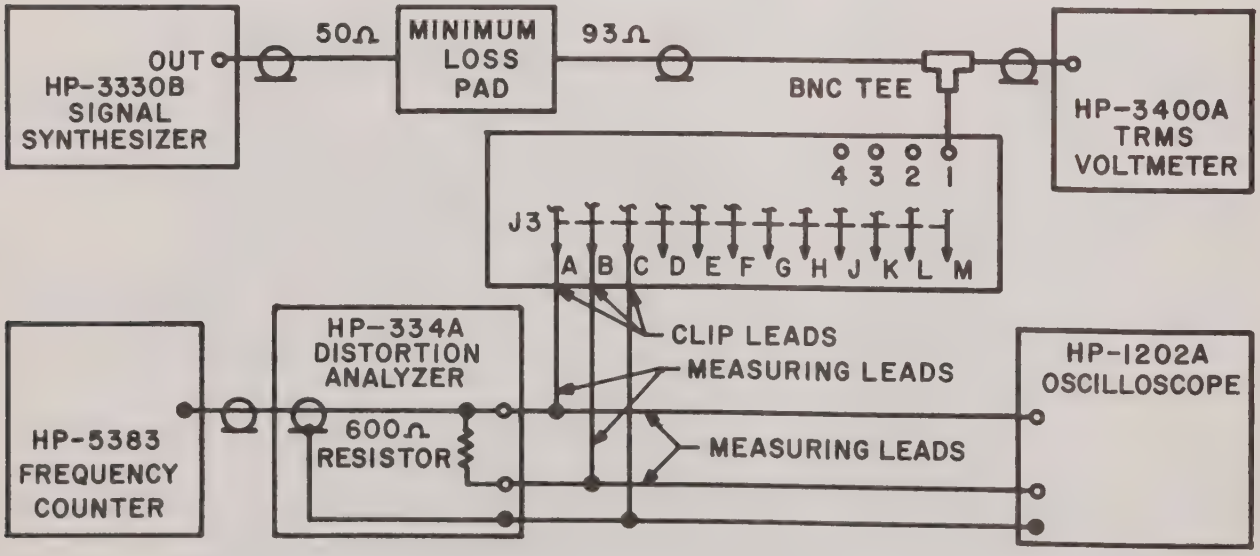


Figure 5-2. Test Setup, Baseband - VF Conversion Test

2. Set signal synthesizer output frequency to 1.0 kHz and output level to 1.71 mV rms as indicated on TRMS voltmeter.

3. Set Demodulator controls as follows:

a.	POWER	- Off
b.	Rear Panel Routing Switches	- BRDG position
c.	DEMODULATOR SELECT	- 1
d.	Phone LEVEL	- Max. CCW

4. Set Demodulator POWER switch to ON position, set all demodulator units to 000.00 kHz, ERECT, and in MANUAL gain mode (adjusted for a nominal -5 dBm as indicated by distortion analyzer in voltmeter mode).

NOTE

The outputs from AUDIO OUTPUT connector J3 are grouped as follows:

1 - A, B, and C (gnd)
2 - D, E, and F (gnd)
3 - G, H, and J (gnd)
4 - K, L, and M (gnd)

5. With clip leads connected to A, B, and C of connector J3, observe oscilloscope and frequency counter indications. The oscilloscope indicates a sine wave at output A, B, and C and the frequency counter indicates 1.000 kHz ±5 Hz.

6. Set demodulator unit to INVERT condition and observe frequency counter indication. The frequency counter indicates 3.000 kHz ±5 kHz.

7. Repeat steps 4 through 6 for the following frequencies:

	Signal Synthesizer Frequency	Demodulator Tuned Frequency
a.	112.110 kHz	111.11 kHz, ERECT
b.	112.110 kHz	111.11 kHz, INVERT
c.	223.220 kHz	222.22 kHz, ERECT
d.	223.220 kHz	222.22 kHz, INVERT
e.	245.440 kHz	244.44 kHz, ERECT
f.	245.440 kHz	244.44 kHz, INVERT
g.	289.880 kHz	288.88 kHz, ERECT
h.	289.880 kHz	288.88 kHz, INVERT
i.	309.000 kHz	308.00 kHz, ERECT
j.	309.000 kHz	308.00 kHz, INVERT

8. Repeat steps 4 through 7 for demodulator units 2, 3, and 4 while connecting clip leads to outputs D, E, and F; G, H, and J; and K, L, and M (respectively, for units 2, 3, and 4).

9. Set signal synthesizer output frequency to 309.000 kHz, tune demodulator unit 1 to 308.00 kHz, connect measuring leads to front panel PHONES output jack, adjust LEVEL control maximum CW, and measure output level. The output level is at least +10 dBm.

10. Repeat step 9 for demodulator units 2, 3, and 4.

11. Set Demodulator POWER switch to off position.

5.2.3.7 Manual and AGC Control Range Test

1. Connect test equipment to Demodulator as shown in Figure 5-3.

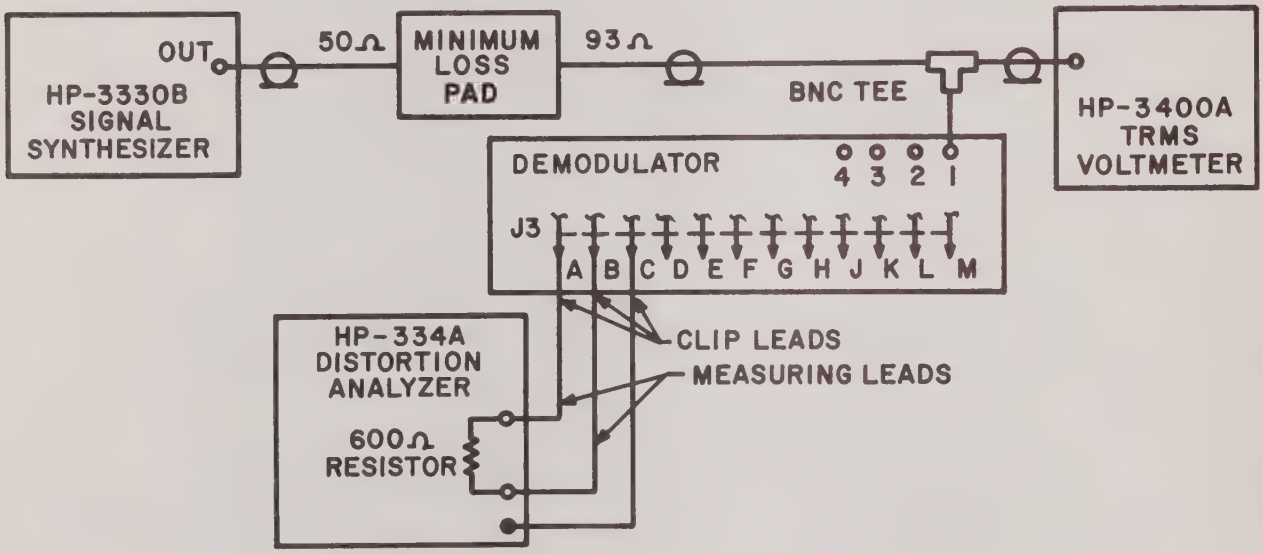


Figure 5-3. Test Setup, Manual/AGC Control Range Test

2. Set signal synthesizer output frequency to 2.000 kHz and output level to 1.71 mV rms as indicated on TRMS voltmeter.

3. Set Demodulator controls as follows:

a.	POWER	- Off
b.	Rear Panel Routing Switches	- BRDG position
c.	Phone LEVEL	- Max. CCW
d.	DEMODULATOR SELECT	- 1

4. Set Demodulator POWER switch to ON position, demodulator unit to 000.00 kHz, ERECT, and in MANUAL gain mode.

5. Using INCR/DECR switch, adjust gain for maximum gain and observe and record VF output level indicated on distortion analyzer.

6. Using INCR/DECR switch, continually adjust gain for minimum gain as observed on distortion analyzer, increase signal synthesizer output level until distortion analyzer indicates VF output level recorded in step 5. The signal synthesizer output level is at least 40 dB greater than level indicated on TRMS voltmeter in step 5.

NOTE

In the following step, wait for demodulator unit output to stablize before recording VF output level.

7. Reduce signal synthesizer output level to 1.71 mV rms, set demodulator unit in AGC mode, and record VF output level indicated on distortion analyzer.

8. Increase signal synthesizer output level to 171 mV rms and record VF output level indicated on distortion analyzer. The indicated VF output level does not exceed 3 dB greater than level recorded in step 7.

9. Repeat steps 5 through 8 for demodulator units 2, 3, and 4 substituting VF outputs D, E, and F; G, H, and J; and K, L, and M (respectively, for units 2, 3, and 4).

10. Set Demodulator POWER switch to off position.

5.2.3.8 Noise and Crosstalk Test

1. Connect test equipment to Demodulator as shown in Figure 5-4.

2. Set Demodulator controls as follows:

a.	POWER	- Off
b.	Rear Panel Routing Switches	- INDEP position
c.	Phone LEVEL	- Max. CCW

3. Set Demodulator POWER switch to ON position, set all demodulator units to 100.00 kHz, ERECT, and AGC mode.

4. Connect clip leads to A, B, and C of connector J3 and measure noise output level on distortion analyzer. The noise output level is -65 dBm, or less.

5. Repeat step 4 for demodulator units 2, 3, and 4 measuring noise output levels at D, E, and F; G, H, and J; and K, L, and M, respectively.

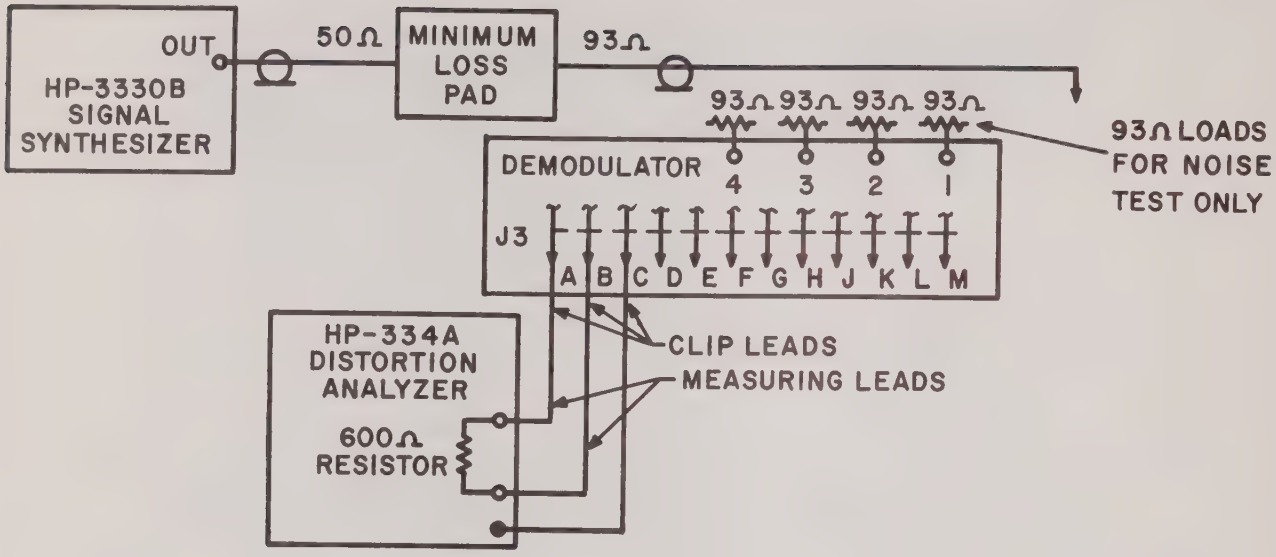


Figure 5-4. Test Setup, Noise and Crosstalk Test

6. For crosstalk test, set rear panel switches S1, S2, and S3 to BRDG positions and connect the signal synthesizer output to demodulator unit 1 input.

7. Set signal synthesizer output frequency to 9.00 kHz and output level to 1.71 mV rms as indicated on TRMS voltmeter.

8. Set demodulator unit 1 to 8.00 kHz, ERECT, at maximum manual gain and record output level on distortion analyzer.

9. Set signal synthesizer output frequency to 7.80 kHz and record output level on distortion analyzer. Output level is at least 45 dB below level recorded in step 8.

10. Set signal synthesizer output frequency to 11.8 kHz and record output level on distortion analyzer. Output level is at least 45 dB below level recorded in step 8.

11. Repeat steps 7 through 11 for demodulator units 2, 3, and 4.

12. Set Demodulator POWER switch to off position.

5.2.3.9 Remote Operational Checkout

Check Demodulator remote operating capability with an IEEE/488 Bus Analyzer by performing the following procedures.

1. Set Demodulator front panel controls as follows:

   a. POWER - Off
   b. DEMODULATOR SELECT - 1

2. Set rear panel voltage selector switch to S2 to match available ac line voltage.

3. Connect IEEE/488 Bus Analyzer to IEEE STD 488 PORT connector J5.

4. Set Demodulator POWER switch to ON position.

NOTE

Ensure REN line is asserted.

5. Using IEEE/488 Bus Analyzer enter the following to Demodulator:

ATN	DATA (BINARY)	DATA (HEX)	ASCII	MEANING	FRONT PANEL VISUAL INDICATION
T	0 0 1 1 1 1 1 1	3F	?	Unlisten	
T	0 1 0 1 0 1 0 1	55	U	Controller, talker	
T	0 0 1 0 0 0 1 1	23	#	9525, listener	
F	0 1 0 0 0 1 0 0	44	D	Demodulator selector	None
F	0 0 1 1 0 0 0 0	30	1	Demodulator unit number	
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return	
F	0 0 0 0 1 0 1 0	0A	LF	Line feed	
T	0 0 1 1 1 1 1 1	3F	?	Unlisten	
T	0 1 0 1 0 1 0 1	55	U	Controller, talker	
T	0 0 1 0 0 0 1 1	23	#	9525, listener	
F	0 1 0 1 0 0 1 0	52	R	Remote mode	RMT indicator lights
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return	
F	0 0 0 0 1 0 1 0	0A	LF	Line feed	
T	0 0 1 1 1 1 1 1	3F	?	Unlisten	
T	0 1 0 1 0 1 0 1	55	U	Controller, talker	
T	0 0 1 0 0 0 1 1	23	#	9525, listener	
F	0 1 0 0 0 1 0 1	45	E	Erect Mode	ERECT indicator lights
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return	
F	0 0 0 0 1 0 1 0	0A	LF	Line feed	
T	0 0 1 1 1 1 1 1	3F	?	Unlisten	
T	0 1 0 1 0 1 0 1	55	U	Controller, talker	
T	0 0 1 0 0 0 1 1	23	#	9525, listener	
F	0 1 0 0 0 0 0 1	41	A	AGC mode	AGC indicator lights
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return	
F	0 0 0 0 1 0 1 0	0A	LF	Line feed	
T	0 0 1 1 1 1 1 1	3F	?	Unlisten	
T	0 1 0 1 0 1 0 1	55	U	Controller, talker	
T	0 0 1 0 0 0 1 1	23	#	9525, listener	
F	0 1 0 0 0 1 1 0	46	F	Frequency ID	
F	0 0 1 1 0 0 0 1	31	1	MSD	

ATN	DATA (BINARY)	DATA (HEX)	ASCII	MEANING	FRONT PANEL VISUAL INDICATION
F	0 0 1 1 0 0 1 0	32	2	-	Numeric display displays 123.21
F	0 0 1 1 0 0 1 1	33	3	-	
F	0 0 1 1 0 0 1 0	32	2	-	
F	0 0 1 1 0 0 0 1	31	1	LSD	
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return	
F	0 0 0 0 1 0 1 0	0A	LF	Line feed	

6. Initiate Demodulator to bus analyzer response by entering:

T	0 0 1 1 1 1 1 1	3F	?	Unlisten
T	0 0 1 1 0 1 0 1	35	5	Controller, listener
T	0 1 0 0 0 0 1 1	43	C	9525, talker

NOTE

The Demodulator to bus analyzer response is:

F	0 1 0 0 0 1 0 0	44	D	Demodulator ID
F	0 0 1 1 0 0 0 1	31	1	Demodulator unit number
F	0 1 0 0 0 1 0 1	45	E	Erect mode
F	0 1 0 0 0 0 0 1	41	A	AGC mode
F	0 1 0 1 0 0 1 0	52	R	Remote mode
F	0 1 0 0 0 1 1 0	46	F	Frequency ID
F	0 0 1 1 0 0 0 1	31	1	MSD
F	0 0 1 1 0 0 1 0	32	2	-
F	0 0 1 1 0 0 1 1	33	3	-
F	0 0 1 1 0 0 1 0	32	2	-
F	0 0 1 1 0 0 0 1	31	1	LSD
F	0 1 0 1 0 1 1 0	56	V	Level ID
F	0 1 0 1 0 1 0 1	55	U	Level (under)
F	0 1 0 0 1 1 0 0	4C	L	Limit or
F	0 0 1 0 0 0 0 0	20	SP	Space
F	0 0 0 0 1 1 0 1	0D	CR	Carriage return
F	0 0 0 0 1 0 1 0	0A	LF	Line feed

Repeat steps 5 and 6 for each remaining demodulator unit, as required, substituting the following in both command and response at Demodulator Unit number:

a. Demodulator Unit 2;

F 0 0 1 1 0 0 0 1 31 1

b. Demodulator Unit 3;

F 0 0 1 1 0 0 1 0 32 2

c. Demodulator Unit 4;

F 0 0 1 1 0 0 1 1 33 3

5.3 CORRECTIVE MAINTENANCE

Corrective maintenance for the Demodulator consists of fault isolation/troubleshooting, repair, alignment/adjustment, and post repair procedures.

5.3.1 GUIDELINES

Demodulators which either fail to meet Performance Standards (Table 5-2) or have operationally identified malfunctions will require corrective maintenance. Troubleshooting and repair of the Demodulator is performed on two levels. The first level involves isolating a fault to a subassembly which can be quickly replaced to return the Demodulator to an operating condition. The second level involves identifying and isolating a fault to a subassembly component and then repairing/replacing that component. Demodulator fault isolation techniques include:

1. An Operationally Identified Fault Symptoms Chart, Table 5-3, is provided to assist routine operations personnel in identifying and correcting major, box-level Demodulator faults.

2. The Performance Tests in paragraph 5.2 will aid maintenance technicians in identifying specific fault symptoms involving defective subassemblies.

3. A Troubleshooting Flow Chart, Figure 5-5, is provided in this paragraph to be used in conjunction with the Performance Tests in paragraph 5.2. Specific test steps within the Flow Chart aid in isolating a fault to a defective subassembly.

4. Demodulator Theory of Operation, Section IV, and Schematic Diagrams, Section VII, are provided to aid the maintenance technician in tracing a fault to a faulty subassembly component.

Table 5-3. Operationally Identified Fault Symptoms

Symptom	Probable Cause/Corrective Action
Totally inoperative; POWER ON lamp and all displays do not light.	1. Fuse F1 or F2 blown. 2. Power cord defective. 3. Check facility power source.
One or more indicators on single demodulator unit do not light.	1. Replace faulty unit.
Failure of one or more indicators on all demodulator units.	1. Replace control unit. 2. Replace control rack frame.
Failure on one or more controls on single demodulator unit.	1. Replace faulty unit.
Failure of one or more controls on all demodulator units.	1. Replace control unit. 2. Replace control rack frame.

Table 5-3. Operationally Identified Fault Symptoms (Continued)

Symptom	Probable Cause/Corrective Action
No VF or Phone output on single demodulator unit.	1. Replace faulty unit.
No VF or Phone output on all demodulator units.	1. Replace control unit. 2. Replace control rack frame.

5.3.2 OPERATOR MAINTENANCE PROCEDURES

Routine operations personnel encountering major Demodulator malfunctions should proceed as follows:

1. Verify that the Demodulator controls are properly set.

2. Verify that all interface cables are connected properly and are not defective.

3. Verify (if possible) that input signals are correct.

4. Refer to the Operationally Identified Fault Symptoms Chart, Table 5-3, to correct a malfunction.

5. Malfunctions traceable to a single demodulator unit may be confirmed by swapping with a good unit in the same rack.

6. Any faults not correctable using these procedures should be referred to a qualified maintenance technician.

5.3.3 TROUBLESHOOTING/FAULT ISOLATION PROCEDURES

To troubleshoot a defective Demodulator, refer to the Troubleshooting Flow Chart, Figure 5-5, and proceed as follows:

1. Begin at START and proceed horizontally through the chart. Perform each indicated Performance Test (referring to paragraph 5.2 for details of each test) until a fault (NO) is encountered.

2. Isolate the fault to a subassembly by proceeding vertically through the troubleshooting path and performing the indicated tests. It will be necessary to use the extender cables and boards supplied with the demodulator to gain access to internal test points.

3. Replace the defective subassembly indicated by the Flow Chart.

4. Verify Demodulator operation by re-performing the Performance Tests in paragraph 5.2.3. Return the Demodulator to service if the results are satisfactory.

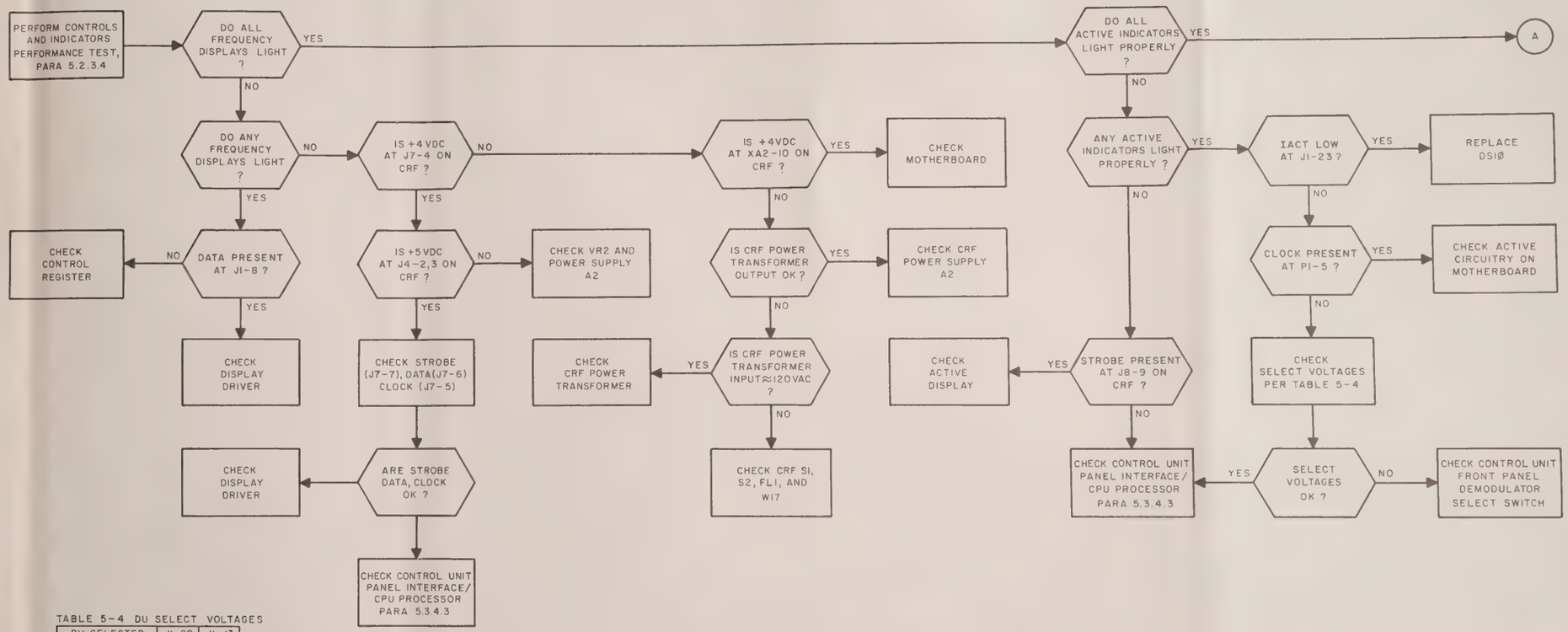


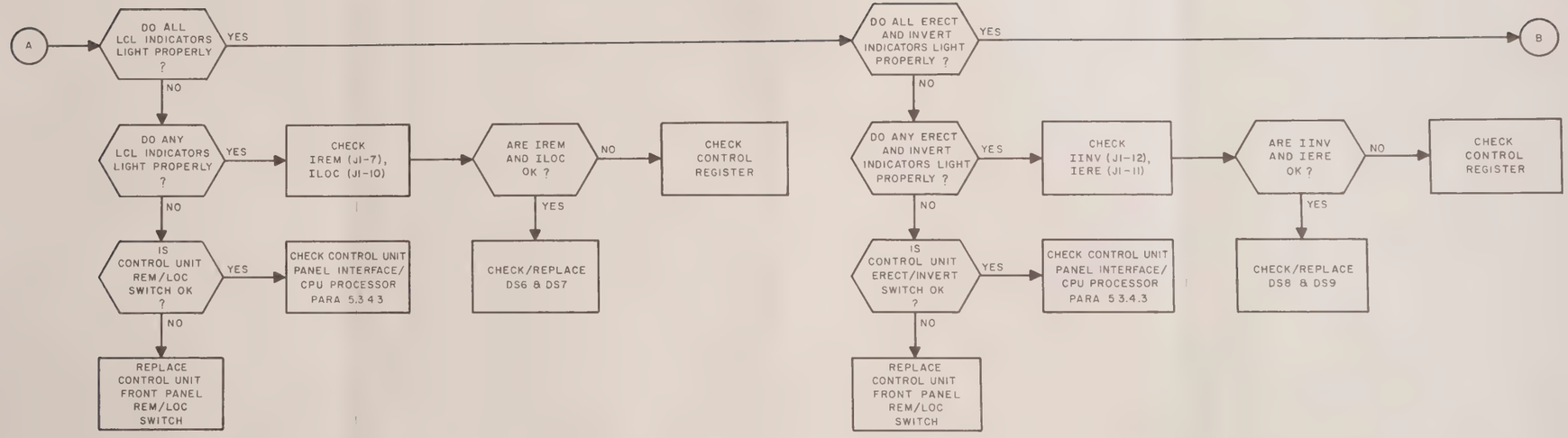
TABLE 5-4 DU SELECT VOLTAGES

DU SELECTED	J1-20	J1-13
#1	L	L
#2	L	H
#3	H	L
#4	H	H

NOTE: L =< 0.5VDC
H => 2.5VDC

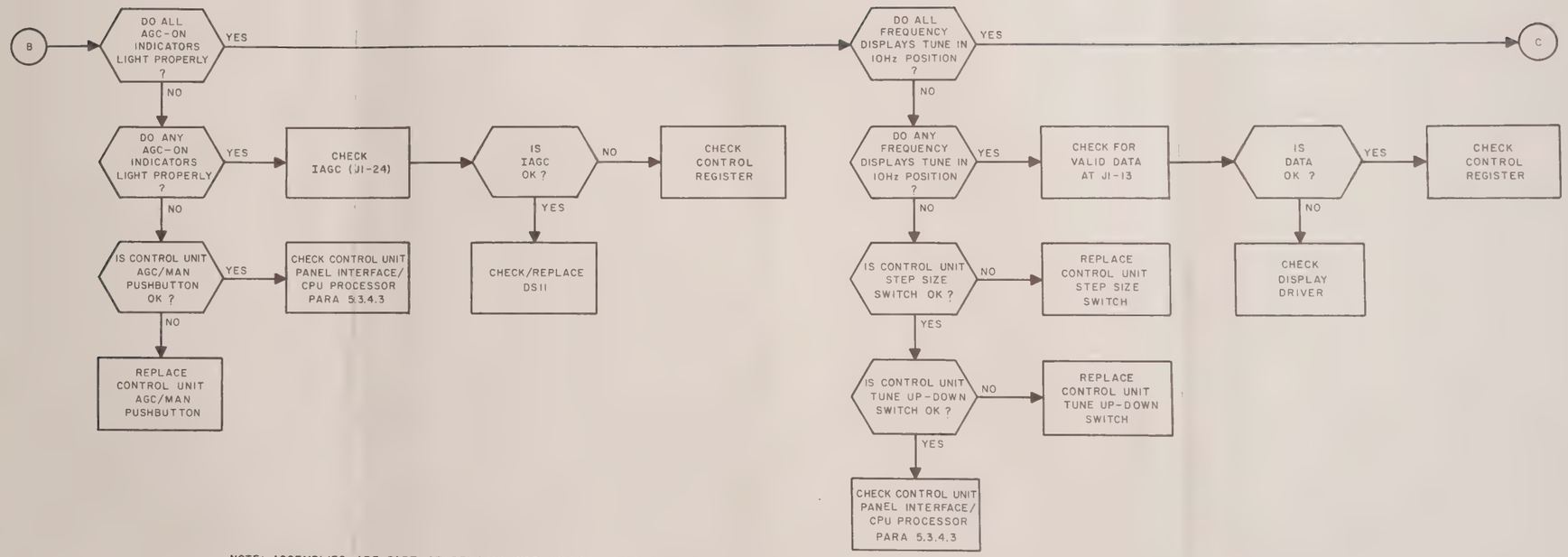
NOTE: ASSEMBLIES ARE PART OF DEMODULATOR UNITS 1 THRU 4 UNLESS OTHERWISE INDICATED

Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 1 of 7)



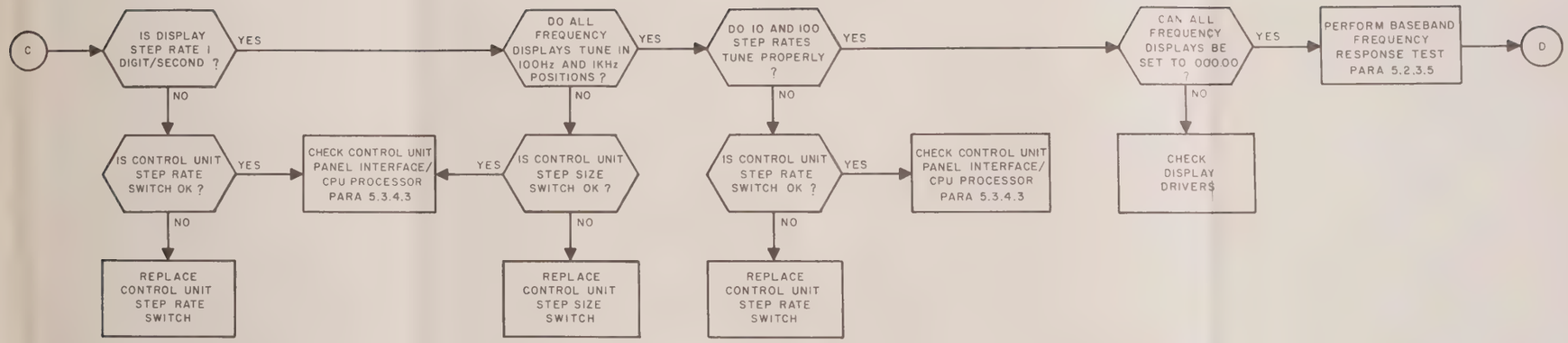
NOTE: ASSEMBLIES ARE PART OF DEMODULATOR UNITS 1 THRU 4 UNLESS OTHERWISE INDICATED.

Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 2 of 7)



NOTE: ASSEMBLIES ARE PART OF DEMODULATOR UNITS 1 THRU 4 UNLESS OTHERWISE INDICATED

Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 3 of 7)


C
IS DISPLAY STEP RATE 1 DIGIT/SECOND ?
YES
NO
DO ALL FREQUENCY DISPLAYS TUNE IN 100Hz AND 1KHz POSITIONS ?
YES
NO
DO 10 AND 100 STEP RATES TUNE PROPERLY ?
YES
NO
CAN ALL FREQUENCY DISPLAYS BE SET TO 00000 ?
YES
NO
PERFORM BASEBAND FREQUENCY RESPONSE TEST PARA 5.2.3.5
D
IS CONTROL UNIT STEP RATE SWITCH OK ?
YES
NO
CHECK CONTROL UNIT PANEL INTERFACE/ CPU PROCESSOR PARA 5.3.4.3
REPLACE CONTROL UNIT STEP RATE SWITCH
IS CONTROL UNIT STEP SIZE SWITCH OK ?
YES
NO
CHECK CONTROL UNIT PANEL INTERFACE/ CPU PROCESSOR PARA 5.3.4.3
REPLACE CONTROL UNIT STEP SIZE SWITCH
IS CONTROL UNIT STEP RATE SWITCH OK ?
YES
NO
CHECK CONTROL UNIT PANEL INTERFACE/ CPU PROCESSOR PARA 5.3.4.3
REPLACE CONTROL UNIT STEP RATE SWITCH
CHECK DISPLAY DRIVERS

NOTE: ASSEMBLIES ARE PART OF DEMODULATOR UNITS 1 THRU 4 UNLESS OTHERWISE INDICATED.

Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 4 of 7)

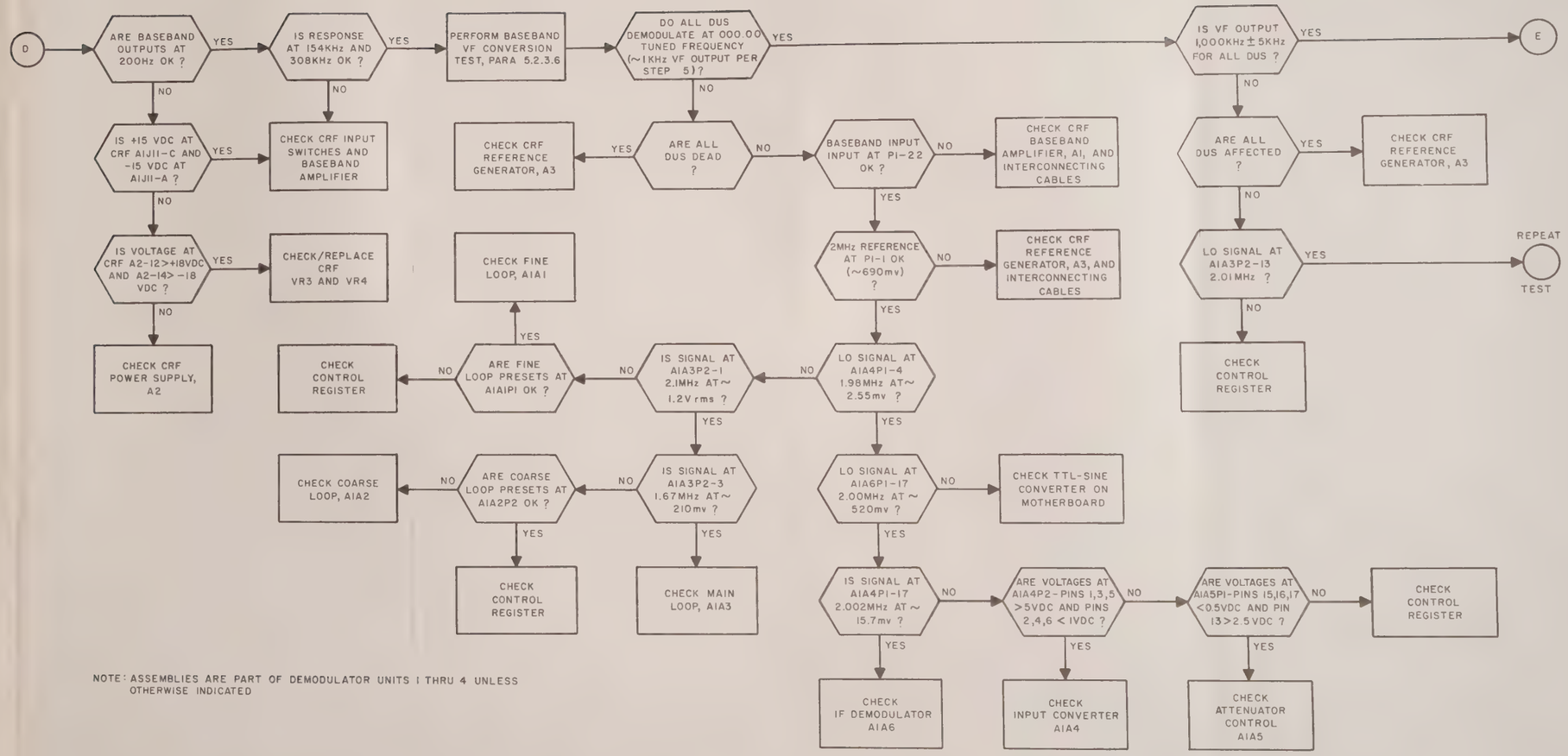


Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 5 of 7)

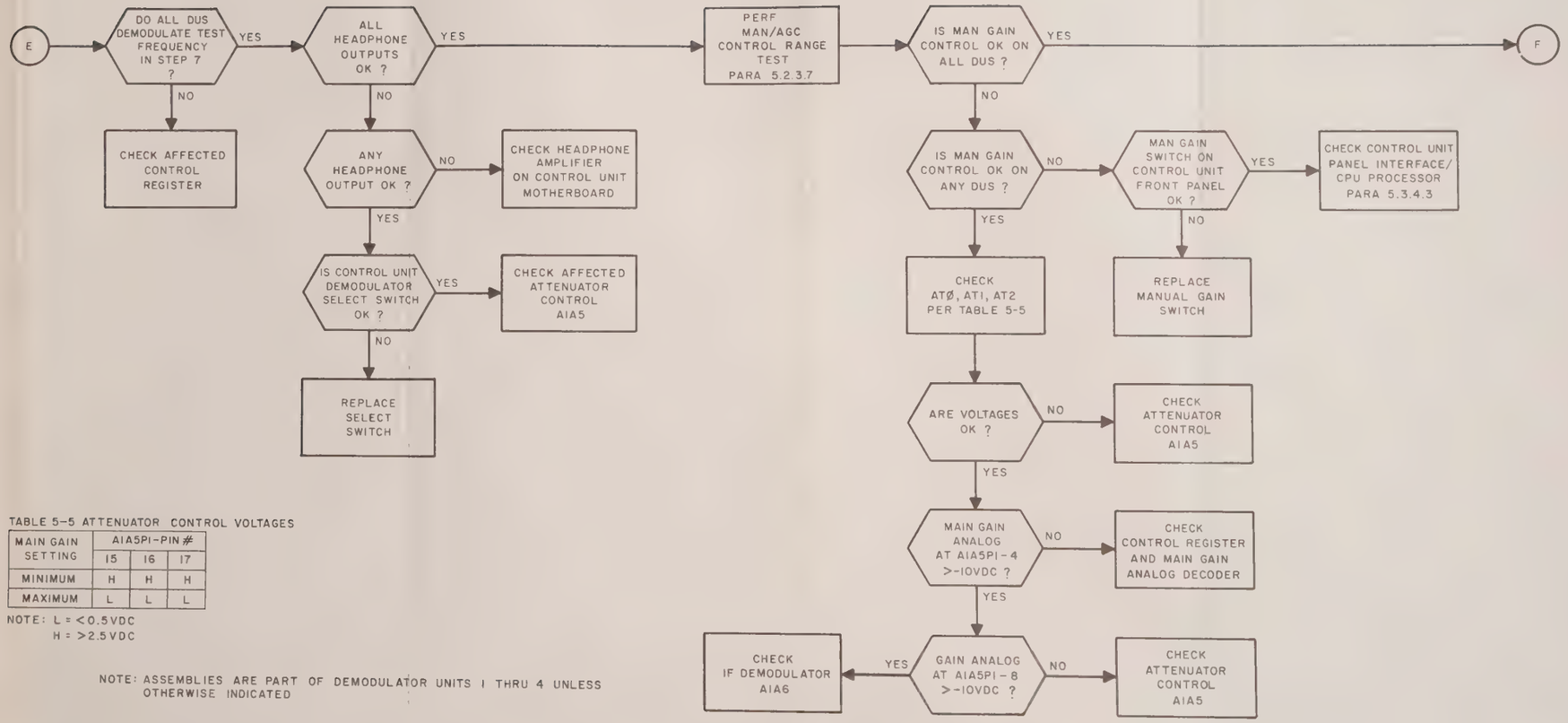


TABLE 5-5 ATTENUATOR CONTROL VOLTAGES

MAIN GAIN SETTING	A1A5P1-PIN #		
	15	16	17
MINIMUM	H	H	H
MAXIMUM	L	L	L

NOTE: L = <0.5VDC
H = >2.5VDC

NOTE: ASSEMBLIES ARE PART OF DEMODULATOR UNITS 1 THRU 4 UNLESS OTHERWISE INDICATED

Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 6 of 7)

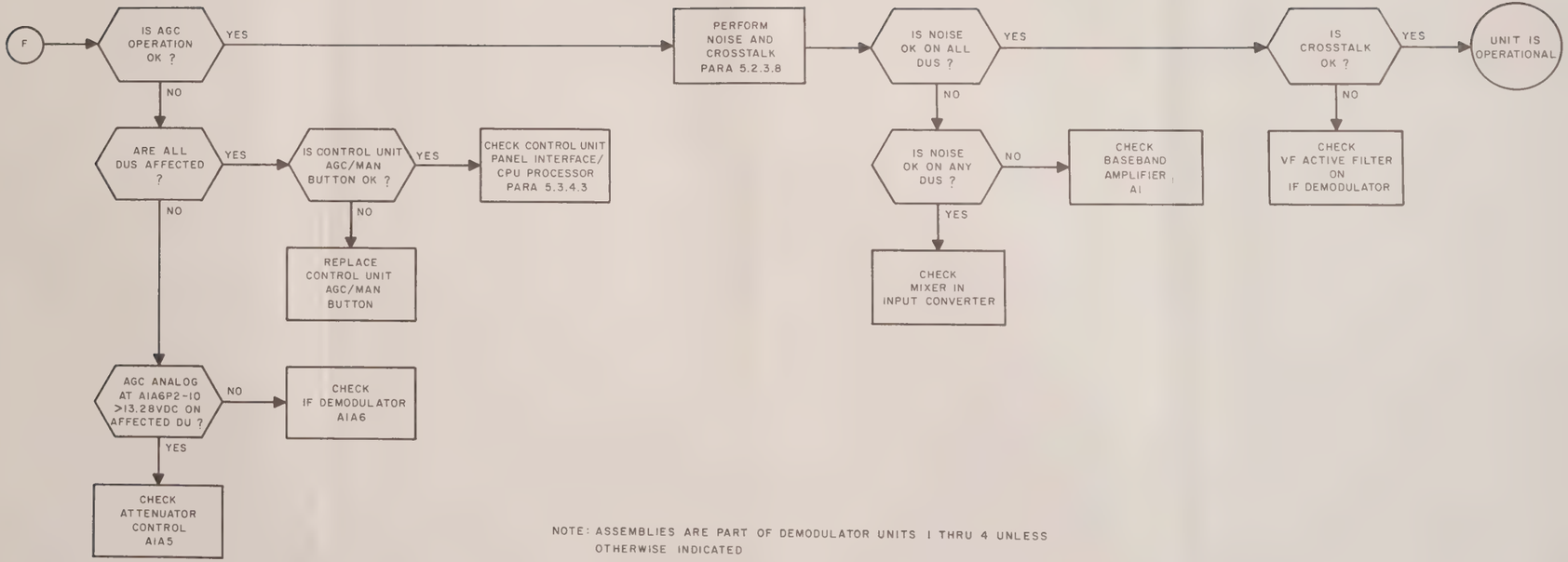


Figure 5-5. Demodulator Troubleshooting Flowchart (sheet 7 of 7)

5. Refer to paragraph 5.3.4 to repair the defective subassembly. Procedures for testing and isolating Front Panel Interface/CPU Processor faults are given in paragraph 5.3.4.3.

5.3.4 SUBASSEMBLY CORRECTIVE MAINTENANCE

5.3.4.1 General

Subassembly troubleshooting includes resistance and dc voltage checks, signal tracing, circuit analysis and component substitution. Because of the complexity and sophistication of digital section components, troubleshooting techniques for the Front Panel Interface/Demod Control and CPU Processor and Memory Modules are presented separately in paragraph 5.3.4.3.

5.3.4.2 Subassembly Fault Isolation Procedures

Demodulator subassembly testing and fault isolation requires the use of a serviceable control rack frame, control unit and plug-in demodulator unit. Test equipment required are listed in paragraph 5.2.3.3. The following guidelines apply to all replaceable subassemblies except digital section components (see paragraph 5.3.4.3).

1. Thoroughly inspect the defective subassembly for burnt or defective components, loose solder connections or any other physical damage.

2. Place the subassembly on an appropriate extender board or cable.

3. Using appropriate test equipment, trace signal flow through the subassembly. Refer to Circuit Description in Section IV and Schematic Diagrams, Section VII, to test and verify the operation of active components and major circuit areas on the subassembly.

4. When a faulty component is identified, replace it using the techniques outlined in paragraph 5.3.5. Verify the subassembly operation by repeating the checks described in step 3 above.

5. Verify correct operation of the demodulator by re-performing the applicable Performance Tests in paragraph 5.2.3.

5.3.4.3 Digital Section Testing

Testing and troubleshooting of digital section components should be performed by technicians experienced in digital circuit techniques and who are familiar with the principles of operation of the Panel Interface/Demod Control and the CPU Processor and Memory Bus as outlined in paragraphs 4.4.2.2 and 4.4.2.1. Minimum test equipment requirements are a high-speed logic probe and a dual-trace, wide-band oscilloscope. The following guidelines are not exhaustive, but are helpful in assisting the technician in tracing data flow through the digital section.

1. Operation of the Panel Interface/Demod Control Module may be checked by operating the front panel switches and tracing each switch's control line through the Module to U4.

2. Check U4 by alternately tying the $\overline{RD}$ and $\overline{WR}$ pins low and observing the movement of data through U4.

3. The operation of gates, multiplexers, buffers and I/O drivers may be checked by tying the applicable input pins high or low through 1 k resistors and looking for the required output state.

4. Check the CPU Processor by presetting (temporarily hard-wiring) data on its input lines and checking for correct data on the serial output. It may be useful to disable the system clock and substitute an external, low-speed clock source to step through the program sequence at a slow rate.

5. Suspected program (ROM) errors may be resolved by single stepping the processor and comparing the ROM data output with the program listing in paragraph 5.3.4.5.

6. In circuit areas where tracing is difficult due to high signal interdependency, troubleshooting may be accomplished by substituting a known good component for a suspected faulty component and then verifying system integrity using the applicable performance test.

5.3.4.4 Program Operation

This paragraph contains the explanation of the program used in Demodulator operation. This paragraph, along with the program listing in paragraph 5.3.4.5, are presented as aids in digital section troubleshooting. Table 5-6 lists the various program operations and their table locations.

Table 5-6. Program Operation

Program Operation	Table Reference
Frequency Tuning, 0 to 308 kHz	5-7
Erect/Invert Selection	5-8
Manually Adjustable Gain/AGC Selection	5-9
Local/Remote Operator Request	5-10
Initialization and Power	5-11
Remote Listener and Talker	5-12
Jump Table	5-13
ASCII Status Conversion	5-14
Operational and Miscellaneous Routines	5-15
Index of Labels and RAM Locations	5-16
Description of Major Routines	5-17

Table 5-7. Frequency Tuning, 0 to 308 kHz

Label	Step	Operation	Proceed to (If Yes)/(If No)
		1. LOCAL (within 'LEVS')	
	a	Tuning switch operated?	b/MGAIN (Table 5-9)
	b	In up position?	TUNUP/TUNDN
TUNUP	c	MSD = 3?	d/AD1
	d	LSD's = ?	EQ8/e
	e	KH3 = 7?	ENDT/AD1
	f	Stepsize = 1 KC?	ENDT/g
	g	LSD = 0?	AD1/h
	h	2nd LSD = 9?	i/AD1
	i	Stepsize = 100's?	ENDT/AD1
EQ8	j	KH3 = 8?	ENDT/AD1
AD1	k	Stepsize = 10's? 1 → B; 3 → C	n/l
	l	Stepsize = 100's? 10 → B	n/m
	m	1 → B; 2 → C	
	n	Clear carry.	
ALOOP	o	Add B (step) to C digits.	IRET
TUNDN	p	3 MSD's = 0?	q/MIN
	q	2 MSD's 0 ?	ENDT/r
	r	Stepsize = KH3 ?	ENDT/s
	s	2 LSD = 0 ?	t/MIN
	t	Stepsize = 100's?	ENDT/MIN
MIN	u	Stepsize = 10's? 1 → B; 3 → C	v/SLOOP
	v	Stepsize = 100's? 10 → B	w/SLOOP
	w	1 → B, 2 → C	
SLOOP	x	Subtract B (step) from C digits.	IRET
IRET	y	Update demodulator (SEND).	
ENDT	z	Restore pre-interrupt status, enable interrupts, return to panel monitor	
		2. REMOTE (from Jump Table 5-13, JTBLT)	
FRQ	a	Get pointer of MSD in demodulator Status.	
	b	Get 2nd byte received in "BIST"; Kill ASCII.	
	c	Merge new MSD with status nibble; store it.	
FR2	d	Set pointers.	
	e	Get next input byte; kill ASCII.	
	f	Rotate and save it in B.	
	g	Get next input byte; kill ASCII.	
	h	Merge with last in B.	
	i	Store it.	
	j	Loop FR2 once more (LSB's).	RCMD (Table 5-13)

Table 5-8. Erect/Invert Selection

Label	Step	Operation	Proceed to (If Yes)/(If No)
		1. LOCAL (within the panel monitor) Set	
ZTF	a	End tuning switch test.	
	b	Extract both Erect/Invert and Man/AGC switches.	
	c	Test for either switch operated.	d/RLD (Table 5-10)
	d	First operation this pass?	e/TSW(Table 5-15) (note 1)
	e	Rotate bit(s) to match status byte position(s)	
	f	Get status byte address.	
	g	Toggle corresponding status bit(s).	
	h	Send new status to demodulator.	TSW (Table 5-15)
		2. REMOTE (from Jump Table 5-13, JTBLT	
ERE	a	Get status byte for this demodulator.	
	b	Zero to bit 5. (0 = Erect)	
IN	a	Get status byte for this demodulator.	
		One to bit 5. (1 = Invert)	RCMD (Table 5-13)

NOTE 1 - If first pass flag set, switch has not yet been released. Wait for release; go to beginning. Insure one status toggle only.

Table 5-9. Manually Adjustable Gain/AGC Selection

Label	Step	Operation	Proceed To (If Yes)/(If No)
		1. LOCAL (Manual gain adjustment. Interrupt response, real time clock.)	
MGAIN	a	Get status byte.	
	b	Mode AGC?	ENDT (Table 5-7)/c
	c	Is gain switch actuated?	ENDT (Table 5-7)/d
	d	'Space' to limit byte, if RDNUM = DNUM.	
	e	Gain up switch operated?	UPTST/f
	f	Gain byte at lower limit?	FIXR/GDN (Table 5-15)
	g	Go to IRET.	
UPTST	h	Gain byte at upper limit?	FIXR/GUP (Table 5-15)
	i	Go to IRET.	
FIXR	j	'L' to limit byte, if RDNUM = DNUM. (Note 1)	ENDT (Table 5-7)
		2. REMOTE (from Jump Table 5-13, JTBLT) Set manual gain and increase or decrease	
MG	a	Get status byte pointer.	
	b	Zero to bit 7 (0 = Manual).	
	c	Get next byte in.	
	d	Byte = ' + ' ?	f/h
	e	'Space' to limit indicator byte.	
	f	Is gain byte at maximum? (No PADS and counter = 1F)	LIM/GUP (Table 5-15)
	g	Go to RCMD.	
DN	h	IS gain byte at minimum? (ALL PADS and counter = 0)	LIM/GDN (Table 5-15)
	i	Go to RCMD.	
LIM	j	Store an "L" at remote gain limit indicator.	RET

NOTE 1 - 'Space' or 'L' indicate the gain byte status in the last character of the remote controller status reply (Byte 14). 'L' indicates that the gain is either maximum or minimum.

Table 5-10. Local/Remote Operator Request

Label	Step	Operation	Proceed To (If Yes)/If No)
		1. REMOTE to LOCAL OPERATOR REQUEST (within the panel monitor).	(Note 1)
RLD	a	Clear 1st pass flag. (MFLG)	
	b	IS service request already pending?	TSW (Table 5-15)/c
	c	Is remote flag (RMFG) already set?	RSW/d
	d	IS LOC/REM switch depressed?	e/ESC
	e	0 to LOC/REM status bit; send.	
	f	Merge SRQ bit with demod. no.	
	g	Output to serial poll register.	
ESC	h	Store A at remote flag (RMFG).	CFLG (Table 5-15)
	i	LOC/REM switch still depressed?	CFLG (Table 5-15)/ESC
		2. LOCAL TO REMOTE OPERATOR REQUEST (within Jump Table 5-13, JTBLT).	(Note 2)
LOC	a	Reset status bit 5 (LOC/REM) to 0 (LOC).	RCMD (Table 5-13)
RE	b	Set status bit 5(LOC/REM) to 1 (REM).	RCMD (Table 5-13)

NOTE 1 - a Clears 1st pass flag for ERE/INV and AGC/MAN change.
b If true, 1st request not serviced yet; ignore.
c If true, switch has been serviced already.
d Is a request bit being made?
e Yes, then 0 (LOC) to bit 5 of status byte.
f,g Output identify for remote controller serial poll.
h Set 1st pass flag to avoid further service.
i If switch is released, clear remote flag (0→RMFG).

NOTE 2 - a Single character received from remote controller was "L" in write command.
b Single character received from remote controller was "R" in write command.

Table 5-11. Initialization and Power Up

Label	Step	Operation	Proceed to (If Yes)/(If No)
		1. INITIALIZE MEMORY (RAM).	
	a	PROM location 0 - Set stack pointer.	PWRUP
PWRUP	b	Power up time delay, decrement A to 0.	
NXT	c	Clear 1st 9 bytes of RAM.	
	d	0 to demod number (DNUM).	
	e	1 to new status word (NSWD).	
	f	Make level bytes false to insure update.	
	g	Make port c = output; A and B = inputs.	
	h	Set 1st level address (EF to 'DAT').	
	i	Set port D for level of demod 0.	
	j	Set real time clock constants (LCNT and MCNT).	
	k	Set repeating mode for timer.	
		2. INITIALIZE 488 COMMUNICATIONS.	
	a	Set 488 device address (ADSW to ADRG).	
	b	Reset 488 chip (AUXO).	
	c	Clear address mask register (ADDM).	
	d	Clear any pending 488 interrupt (INST).	
	e	Enable byte in and byte at interrupts (INTM).	
	f	Clear interrupts again.	
	g	Initialize input and output pointers (IBAS and OBAS).	
	h	'Space' to 'L' ; remote gain limit indicator blank.	
	i	Is memory check byte = AA?	COR1/ERO
		3. SETUP DEMODS WITH MEMORY STATUS.	
COR1	a	Set up for local mode at power up.	
FLOC	b	Force local on all demods (0 to status bytes, bit 5).	
CORR	c	Set up for total demods in chassis.	
NXTI	d	Send memory status to a demod.	
	e	Repeat step d for all demods.	
ENAB	f	Enable 7.5 and 6.5 interrupts.	
	g	Enable interrupt activity.	CFLG (Table 5-15)
		4. INITIALIZE DEMOD MEMORY DATA on POWER UP RAM FAIL.	
ERO	a	Set status pointer and total demod counter.	
ER1	b	Get initial data status pointer and byte counter.	
ER2	c	Initialize status of all demods.	
NEXD	d	Do step c for all demods.	OK
OK	e	Set power up flag to indicate good RAM (AA → MEMCK).	COR1

Table 5-12. Remote Talker and Listener

Label	Step	Operation	Proceed to (If Yes)/(If No)
		(RESPONSE TO INTERRUPT 6.5) PROM LOCATION 34 HEX.	
TST1	a	Is 488 status a listener?	LINT/b
	b	A talker?	BTALK/ENDT (Table 5-7)
LINT	c	Get byte in pointer (IBAS).	
IDAT	d	Byte in interrupt true?	e/IDAT
	e	Get 488 input data byte; store it.	
	f	Increment and store pointer.	
	g	Is input character the terminator? (Line Feed)	JTBLT (Table 5-13)/ ENDT (Table 5-7)
BTALK	h	Is byte out buffer full?	BTALK/i
	i	Clear serial poll output.	
	j	Get output byte pointer (OBAS).	
	k	Output data to remote controller.	
	l	Increment and store pointer.	
	m	Is this the terminator character?	LBYT/ENDT (Table 5-7)
LBYT	n	Reset the data out pointer.	
	o	Clear last data out interrupt.	ENDT (Table 5-7)

Table 5-13. Jump Table

Label	Step	Operation	Proceed to (If Yes)/(If No)
		JUMP TABLE (Note 1)	
JTBLT	a	Reset data input pointer (IBAS).	
	b	Is the first byte received a "D"?	DEMN/c
	c	Is the present demod in remote?	REMT/d
	d	Is the first byte received a "R"?	REMT/LOC (Table 5-10)
REMT	e	Then is the character in the table? (CHT)	CJT/f
LP1	f	Try the next and increment counter.	REMT
CJT	g	Multiply counter x3: add to JTBL.	
JTBL	h	Go to corresponding routine.	
DEMN	i	Get next input character, kill ASCII.	
	j	Store at remote demod indicator (RDNUM).	
	k	Same demod as locally selected? (= DNUM)?	ASCII (Table 5-14)/1
	l	Set NSWD to force local demod update.	ASCII (Table 5-14)
RCMD	m	Make DNUM equal to RDNUM.	
	n	Set demod change flag (DDEM).	
	o	Get demod statud pointer (TDEM).	
	p	Send updated status to demod. (SEND).	ASCII (Table 5-14)

NOTE 1 - Other jumps:
LOCAL (LOC) - Table 5-10,
FRQ - Table 5-7,
ERE/INV - Table 5-8,
AGC/MAN - Table 5-7, Table 5-8

Table 5-14. ASCII Status Conversion

Label	Step	Operation	Proceed to (If Yes)/(If No)
		CONVERTS PRESENT DEMOD STATUS TO ASCII FORMAT STRING TO BE SENT TO THE REMOTE CONTROLLER ON 488 BUS.	
ASCII	a	Get the byte out pointer (FBYTO).	
	b	Store a "D" in the first byte.	
	c	Make RDNUM ASCII, store in second byte.	
	d	Present status AGC?	AG/e
	e	Store "M" in byte 3.	g
AG	f	Store"A" in byte 3.	
	g	Is present status erect?	NER/n
	h	Store"E" in byte 4.	10
NER	i	Store"I" in byte 4.	
	j	Is present status remote?	RT/k
	k	Store"L" in byte 5.	m
RT	l	Store"R" in byte 5.	
	m	Store"F" in byte 6.	
	n	Convert MSD of frequency to ASCII; store byte 7.	
	o	Point second and third MSDs.	
FRQ1	p	Convert two digits to ASCII; store next two bytes.	
	q	Repeat step p for LSBs.	r
	r	Store"V" in byte 12.	
	s	Set counter and base level address.	
CAL	t	Rotate and test for proper address.	MSK
MSK	u	MASK address for level and output it.	
	v	Loop for delay.	
	w	Get this demod's present level (PORT E).	
	x	Replace the previously selected level address (DAT).	
	y	Set up for decimal level calculation.	
	z	Is level byte = 0?	UND/RONC
RONC	aa	Rotate and increment test; compute decimal level.	ac
UND	ab	Store"U" in byte 13.	af
	ac	Make decimal level in eights complement.	
	ad	Is it = 1?	OVR/ae
	ae	Make it ASCII and store byte 13.	
	af	Store "0D" in byte 15.	
	ag	Store "0A" in byte 16.	ENDT (Table 5-7)
OVR	ah	Store "O" in byte 13.	af

Table 5-15. Operational and Miscellaneous Routines

Label	Step	Operation	Proceed to (If Yes)/(If No)
		1. NON-INTERRUPT DEPENDENT (CFLG, TST, STAT)	
CFLG	a	Store 0 at the first flag pass (MFLG).	
TSW	b	Compare the demod select switch to last (NSWD).	
	c	Are they still the same?	d/DNO
	d	Is this demod in remote mode?	RLD (Table 5-10)/e
STAT	e	Is frequency adjust switch active?	f/ZTF (Table 5-8)
	f	Is this the first request (TNFLG = 0)?	g/ZTF (Table 5-8)
	g	Make interrupt counter short. (1 to COUN).	ZTF (Table 5-8)
		(DNO)	
DNO	a	Rotate demod select switch for DNUM (0-3).	
	b	Make three's complement and store DNUM (3-0).	
	c	Set up the status pointer (call TDEM).	
	d	Set delta demod flag (DDEM).	
	e	Return.	SEND
		(RAZE)	
RAZE	a	Convert step size switch to STSIZ flag.	
	b	Get rate flag set based on rate switch.	
	c	Return.	
		(TDEM)	
TDEM	a	Demod number (0-3) times 8 to demod pointer (DPTR).	
	b	Present band switch to BAND flag.	
	c	Return.	
		(GST)	
GST	a	Get the demod pointer byte (DPTR).	
	b	Increment 3 times for status byte in HL.	
	c	Return.	
		(SEND, MOD, NCHG, CLB, SBIT, BIT, NBYT, CLK)	
SEND	a	Has a new demod been selected (DDEM = 0)?	b/MOD
	b	Set 'strobe' line true. (Port C, bit 5 = 0)	
	c	Toggle 'clock' true, then false. (0 to 1 to 0) (clears all ACTIVE indicators).	
	d	Set DDEM = 0.	
MOD	e	Is present demod status erect?	ERECT/INVERT
	f	Is the band switch the same as before?	NCHG/g
	g	Set MSB of status byte to 0.	CLB

Table 5-15. Operational and Miscellaneous Routines (Continued)

Label	Step	Operation	Proceed to (If Yes)/(If No)
NCHG	h	Set MSB of status byte to 1.	
CLB	i	Compute 'clock' bit from DNUM to B.	
	j	Set demod status pointer and byte counter.	
SBIT	k	Get byte, LSB to A, complement, output Port C.	
BIT	l	Call clock.	
	m	Decrement bit counter; = 0?	NBYT/n
	n	Rotate next bit to bit 0.	BIT
NBYT	o	Last byte out?	p/SBIT
	p	Send 'strobe' to latch data in demod.	
	q	Return.	
CLK	r	Merge data and clock bits.	
	s	Reset clock bit; reset all bits.	
		(ERECT, STRB)	
ERECT	a	Convert two LSDs to binary; store at FA and FB.	
	b	Store FC same as third LSD.	
	c	Get two MSDs and (convert to binary) complement.	
	d	Subtract from offset constant ('DB') hex. ('3A')	
	e	Store as CA and CB; set B = 3.	
	f	Compare and derement B for band switch.	
STRB	g	Point to band switch byte, justify, and save band switch in B.	
	h	Get byte with upper nibble zeroed.	
	i	Merge band switch and CC(1) and store byte.	
	j	Return.	
		(BCDBN)	
BCDBN	a	Convert two digit decimal number in A to binary equivalent in A and L.	
	b	Return.	
		(INVERT, ST0, TWO, ELEV, NZRO)	
INVERT	a	Get two LSDs.	
	b	LSDs = 0?	ST0/c
	c	Convert to binary; hundred's complement.	
	d	Store as FA and FB.	
	e	Store at F0 flag (0 or not 0).	
	f	Are 3 LSDs greater than 350?	Set CY/Reset CY
	g	Save the processor status word (PSW).	
	h	Get and justify two MSDs.	
	i	Convert to binary.	
	j	Add offset ('E1' '46'* hex) and carry from PSW.	
	k	Store as CA and CB.	

Table 5-15. Operational and Miscellaneous Routines (Continued)

Label	Step	Operation	Proceed to (If Yes)/(If No)
	l	(Add 0 and carry, then justify for CC) (not Required).	
	m	Store CC (as 2).	
	n	(Is CC = 1?) (Not Required)	o/TWO
	o	CA and CB ('F3' '63'*) hex?	TWO/p
	p	Set band switch = 1.	r
TWO	q	Set band switch = 2.	
	r	Store band switch.	
	s	Get third MSD.	
	t	Carry set in PSW.	ELEV/u
	u	Subtract third LSD from 7; save in B.	
	v	LSDs = 0?	w/NZRO
	w	Increment B.	NZRO
		* 'xx' refers to new L.O. unit.	
ELEV	x	Subtract B from 11 hex.	
	y	Are LSDs = 0?	z/NZRO
	z	Increment B	
NZRO	aa	Save MSN of memory byte. (Band switch and cc).	
	ab	Merge with B (FC) and store byte.	
	ac	Return.	
		(GUP, LAST, MING, MIN1, NP1, NP2,NP3)	
GUP	a	Is counter at upper limit?	MING/b
	b	Increment counter; merge with same pads.	
	c	Store as new gain byte.	
	d	Return.	
MING	e	Are all pads out?	LAST/MIN1
MIN1	f	Are all pad in? (24 dB)	NP3/g
	g	Pads 2 and 3 in? (18 dB)	NP2/h
	h	Pads 1 and 2 in? (12 dB)	NP1/i
	i	Set gain byte to lower limit. (No pads)	
	j	Return.	
NP1	k	Set gain byte to pad 1 and lower limit (LL).	
	l	Return.	
NP2	m	Set gain byte to pads 1 and 2 and LL.	
	n	Return.	
NP3	o	Set gain byte to pads 2 and 3 and LL.	
	p	Return.	

Table 5-15. Operational and Miscellaneous Routines (Continued)

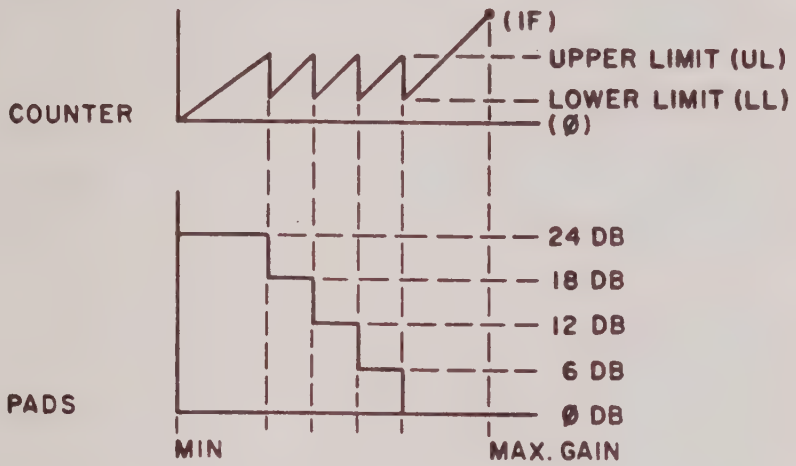
Label	Step	Operation	Proceed to (If Yes)/(If No)
			
		(GDN, GUP1, PAD, PP2, PP3, PP4, GZRO)	
GDN	a	Counter at lower limit?	PAD/b
GUP1	b	Decrement counter; merge with same pads.	
	c	Store as new gain byte.	
	d	Return.	
PAD	e	All pads in? (24 dB)	GZRO/f
	f	Pads 2 and 3 in? (18 dB)	PP4/g
	g	Pads 1 and 2 in? (12 dB)	PP3/h
	h	Pad 1 only in? (6 dB)	PP2/i
	i	Set gain byte to pad 1 and upper limit (UL).	
	j	Return.	
PP2	k	Set gain byte to pads 1 and 2 and UL.	
	l	Return.	
PP3	m	Set gain byte to pads 2 and 3 UL.	
	n	Return.	
PP4	o	Set gain byte to all pads and UL.	
	p	Return.	
GZRO	q	Merge counter with all pads. (Allows decrement of counter to 0.	GUP1
		(RST 65)	
RST65	a	Save present machine status.	
	b	Go to TST1 (Table 5-12).	
		2. INTERRUPT DEPENDENT (RST 75)	
RST 75	a	Save present machine status.	
	b	Go to LEVS.	

Table 5-15. Operational and Miscellaneous Routines (Continued)

Label	Step	Operation	Proceed to (If Yes)/(If No)
		(LEVS, PROC)	
LEVS	a	Is level updat interrupt counter = 0?	NLEV/PROC
PROC	b	Is frequency tuning and manual gain Counter = 0?	c/ENDT
	c	Present status remote?	ENDT/d
	d	Set stepsize and rate flags (RAZE).	
	e	Frequency up/down switch active?	f/MGAIN
	f	Switch in tune up position? TUNDN (Table 5-7)	TUNEUP (Table 5-7)
	g	IRET.	
		(NLEV, RINC, RDAT)	
NLEV	a	Get level at port E.	
	b	Compute last level read address (LLEV).	
	c	Is level same as last time?	RDAT/d
	d	Store this new level at LLEV.	
	e	Is level byte = 0?	g/RINC
RINC	f	Convert level to BCD equivalent in C.	h
	g	Put 8 in C. (Under BCD)	
	h	Merge C with address nibble of DAT.	
	i	Output it to level/address port D.	
	j	Clock the address gate with SOD; rotate DAT.	
RDAT	k	Is DAT rotated to limit (7F Hex)?	l/m
	l	Restore to EF Hex.	
	m	Store new DAT; output new level address.	
	n	Go to Proc.	

Table 5-16. Index of Labels and RAM Locations

Location	Label	Description
2007	BAND	Flag byte storing the current band switch. Tested against each Erect-Invert conversion to enable toggle of bit 7 of the active demodulator unit's status byte as a change in band switch is encountered. Set by the 'TDEM' routine, Table 5-15. 1 byte.
2002	COUN	Counter used for determining the time required between each update for tuning and manual gain adjustment based on the position of the "Rate" switch. It is set in the 'RAZE' subroutine, Table 5-15, and in the panel monitor at first actuation. 1 byte.
2008	DAT	Initialized in 'PWRUP', Table 5-11, to EF Hex. The '0' bit is used to select the first demodulator unit's level latch. At every other 7.5 interrupt, the 'level' of that demodulator unit is read, converted to decimal, and outputted to the demodulator unit's level latch. DAT is then rotated to address the next demodulator unit. It must then be reset to EF Hex when the '0' rotates out to the left to change from demodulator unit 4 to demodulator unit 1. 1 byte. (Used in Table 5-14 and NLEV subroutine, Table 5-15.)
2005	DDEM	Flag byte used in the 'SEND' routine, Table 5-15, to indicate that a new demodulator unit has been selected. (DDEM 0). The byte, if not 0, flags the routine to clear all 'Active' indicators by sending a 'clock' bit while 'strobe' is true. The byte is set in DNO, Table 5-15, and RCMD, Table 5-13, and reset by SEND. 1 byte.
2015	DNUM	Indicates the 'active' demodulator unit number (0 - 3). Set locally in DNO and remotely in RCMD. 1 byte.
2016	DPTR	Demodulator unit pointer is set in the TDEM subroutine, Table 5-15, to the first byte of the selected demodulator unit's status. 2 bytes.
2018, 2037	DST	Demodulator unit status base address. Label for the first status byte 2037 of demodulator unit 1. Used in TDEM subroutine, Table 5-15. 32 bytes.
200D	F0	Flag byte in the INVERT conversion subroutine, Table 5-15, in determining the 0 or non 0 status of the LSDs of tuned frequency. 1 byte.
2038, 2042	IBAS	Base pointer of storage area used for the input data from the BLIST routines. Initialized in PWRUP to FBYTI (2038 Hex). 2 bytes.
2009, 200C	LLEV	Last 'level' reading for corresponding demodulator unit used for comparison each pass through NLEV, Table 5-15. The levels are not updated unless a change in level occurs. Initialized to false values in PWRUP and updated (if required) in NLEV. 4 bytes.

Table 5-16. Index of Labels and RAM Locations (Continued)

Location	Label	Description
200E	MEMCK	Memory check byte used by PWRUP to determine memory integrity indicating no battery failure since last power down. If found invalid, all demodulator units are initialized to Local, Erect, AGC, and frequency = 0. Compared with MEMFG (Hex AA). 1 byte.
2000	MFLG	Flag byte used by the panel monitor to indicate that an operated pushbutton for toggling a function (as AGC/MAN) has already been serviced, and the switch has not yet been released. 1 byte.
2014	NSWD	New status word used to hold the last demodulator selector switch status, and compared against the switch each pass through TSW. Ranges from 0 (demodulator unit 4) to 3 (demodulator unit 1). 1 byte.
2012, 2013	OBAS	Base pointer for ASCII data storage. Used as the variable pointer in the BTALK routine. Initialized in PWRUP to FBYTO (2042 Hex). 2 bytes.
2006	RDNUM	Remote demodulator unit number. Used as the demodulator unit number (DNUM) during remote status request operations in JTBLT. 1 byte.
2003	RMFG	Flag byte used by the panel monitor in RLD to indicate that the Local/Remote switch, although still operated, has been serviced in a previous pass. Byte = 0 when switch is released. 1 byte.
2001	TLTIM	Level service timer. Each time this byte = 0, the next demodulator unit's level indicator is updated if required by NLEV. And, the byte is again set to two counts. 1 byte.
2004	TNFLG	Tuning flag used in STAT to set the timer to minimum on the first pass, so that an immediate change in frequency (based on Up/Down and Stepsize) is observed even at the 1 second rate. This is achieved by setting COUN = 1 on the first pass only, after which, COUN is reset by the RAZE subroutine, Table 5-15. 1 byte.

Table 5-17. Description of Major Routines

Routine	Description
ASCII	Immediately following the last data byte from a remote controller, this routine is invoked to update the ASCII status data used to return the current demodulator status during the basic talker function. The 16 bytes required are stored at FBYTO, Table 5-14.
BTALK	If the control unit is placed in the basic talker mode, each 6.5 interrupt invokes this routine which outputs the data (status) to the remote controller via the 488 interface terminating on a line feed character, Table 5-12.
CFLG	The introduction to the front panel monitor, this routine is the normal recycling start point if no switches are active on the panel. It clears a 'first pass' flag (MFLG), indicating release of a pushbutton function, Table 5-9.
COR1	Following any 'powerup', this routine is used to update the four demodulator units by sending a valid data stream to each unit, Table 5-11.
ENDT	This interrupt is invoked when no change of status is made to a demodulator unit in tuning and manual gain. It bypasses the SEND routine to update the unit, Table 5-7.
ERECT	This subroutine converts the selected decimal frequency, observed on the demodulator unit display, to the binary equivalent data and band switch required in the demodulator data stream for tuning the first LO to the erect mode, Table 5-15.
ERO	If the RAM check byte is not a Hex 'AA' following a 'power up' sequence, RAM is assumed invalid and this routine sets all demodulator units to an initial status of: Local, Erect, AGC, and a base frequency of 000.00 kHz. This occurs after battery failure or removal and reinstallation of the control unit CPU board. The routine precedes COR1, if required, at power up, Table 5-11.
GDN	This subroutine is used to adjust the manual gain byte accounting for 5 bits of gain counter and 3 bits of Pads. The gain is adjusted in a decreasing direction until the counter is zeroed, and all pads are inserted; E0 Hex, Table 5-15.
GUP	The opposite from the GDN subroutine; the manual gain byte is adjusted in an increasing direction until the counter reaches its limit of IF Hex, and all pads are out, 1F Hex, Table 5-15.
INVERT	This subroutine converts the selected decimal frequency, observed on the demodulator unit display, to the binary equivalent data and band switch required in the demodulator data stream for tuning the first LO to the invert mode, Table 5-15.
IRET	The interrupt 7.5 return point following a frequency or manual gain alteration, requiring update of the associated demodulator unit with the SEND subroutine, Table 5-7.

Table 5-17. Description of Major Routines (Continued)

Routine	Description
JTBLT	Following the receipt of a valid message from a remote controller (End of BLIST), this routine is invoked to point to the routine(s) required to fulfill the request in updating the selected demodulator unit. The routine is based on a jump table, Table 5-13.
LINT	The basic listener response to an interrupt 6.5. This routine inputs one byte of data per interrupt, tests for the end of message, and is indicated by a line feed character, Table 5-12.
LEVS	This 7.5 interrupt response routine decrements the level update timer, and tests for 0. If 0, go to NLEV, if not go to PROC.
MGAIN	This interrupt 7.5 response routine checks for valid operation of the manual gain switch, and calls the appropriate subroutine (GUP/GDN) monitoring the gain byte limits. It also sets the remote message gain limit ('L') byte at the upper and lower extremes, Table 5-9.
NLEV	This interrupt 7.5 response maintains the level indicator of each demodulator unit on a rotating basis from 1 to 4 while recycling at an approximate 30 millisecond rate, Table 5-15.
PROC	Interrupt 7.5 response tests the local requirement for manual gain adjustment and points to MGAIN or; manual tuning request pointing a TUNUP or TUNDN as required, Table 5-15.
PWRUP	The power up routine initializes RAM, the 8155 I/O chip, the 488 chip, and the demodulator data stream. It is invoked only at power up, Table 5-11.
RST65	Interrupt vectored response to a remote controller based interrupt, introducing either BTALK or BLIST responses.
RST75	Interrupt vectored response to the real time clock interrupt generated by the 8155 I/O timer, used to service levels, and freuency or manual gain adjustment.
SEND	This major subroutine is invoked following any change of status to a demodulator unit and uses Port C of the 8155 to generate a 56-bit data stream to the selected unit, latching that data in the selected unit. The ERECT or INVERT subroutines are called previous to the data stream. The data stream is sent LSB first from the appropriate 7 bytes held in RAM status. Base DST.
TST1	Following a 488 generated interrupt 6.5, this test points to BLIST or BTALK routines as required, Table 5-15.
TSW	The test switch routine which continually scans for local status change request via the front panel switches, Table 5-15.

Table 5-17. Description of Major Routines (Continued)

Routine	Description
TUNDN	This subroutine subtracts the proper single increment from the decimal frequency value based on the position of the step size switch, Table 5-7.
TUNUP	This subroutine adds the proper single increment to the decimal frequency value based on the position of the step size switch, Table 5-7.

5.3.4.5 Program Listing

The following program listing displays ROM address and corresponding data at that address.

```
                ****************************************
                *WJ-9525 PANEL MONITOR
                *RAM CONSTANTS & FLAGS.
                ****************************************

0000                    ORG   X'2000'
2000            MFLG    DS    1          *1ST PASS FLAG.
2001            TLTIM   DS    1          *LEVEL TIMER.
2002            COUN    DS    1          *TUN/MGAIN TIMER.
2003            RMFG    DS    1          *REM. CONTROL FLAG
2004            TNFLG   DS    1          *TUNE FLAG.
2005            DDEM    DS    1          *DEM. CHGE FLAG.
2006            RDNUM   DS    1          *REMOTE DNO.
2007            BAND    DS    1          *BAND SW. INDIC.
2008            DAT     DS    1          *LEV. ADDR. FLAG.
2009            LLEV    DS    4          *LAST LEVEL DATA.
200D            FO      DS    1          *LSB INDICATOR.
200E            MEMCK   DS    1          *=AA, VALID RAM.
200F            STSIZ   DS    1          *STEP SIZE FLAG.
                *                        *BIT0   10HZ.
                *                        * " 1  100HZ.
                *                        * " 2 1000HZ.

2010            IBAS    DS    2
2012            OBAS    DS    2
2014            NSWD    DS    1          *LAST PORTA DATA.
2015            DNUM    DS    1          *PANEL DEM. NO.
2016            DPTR    DS    2          *STAT. ADDR /DNUM.
2018            DST     DS    32         *STAT. DEMODS,0-3
00AA            MEMFG   EQU   X'AA'      *VALID CHK. BYTE.
0000            PORT0   EQU   0          *CMD/STAT, 8155.
0001            PORTA   EQU   1          *A, 8155.
0002            PORTB   EQU   2          *B,  "
0003            PORTC   EQU   3          *C,  "
0040            PORTD   EQU   X'40'      *LEVEL/ADDR. PORT.
                *       0 TO 3=BCD LEVEL
                *       4 TO 7=SEL DEMS. 1 TO 3.

0060            PORTE   EQU   X'60'      *DECIMAL LEVEL IN.
0004            PORT4   EQU   4          *MODE/LSB, COUNTER
0005            PORT5   EQU   5          *MSB, 8155    "
20FF            STKPT   EQU   X'20FF'
00FF            LCNT    EQU   X'FF'
0027            MCNT    EQU   X'27'
0004            TOTD    EQU   4          *NO. OF DEMODS.
0030            SIM     EQU   X'30'
0020            RIM     EQU   X'20'
00E0            P4      EQU   X'E0'      *24 DB. PAD
00C0            P3      EQU   X'C0'      *18 DB. PAD.
0060            P2      EQU   X'60'
0020            P1      EQU   X'20'
0016            UL      EQU   X'16'      *UPPER LIM, GAIN.
000D            LL      EQU   X'0D'      *LOWER LIM, GAIN.
                ****************************************
                *       IEE95.
                *       BTALK- BASIC TALKER, 8080.
                *       BLIST-   "   LISTENER  "
```

```
                    *           EQUATE LIST
                    *       IEEE 488 REGISTER ADDRESSES.
                    *
                    ************************************
0030                INTM    EQU  X'30'      *INTERRUPT MASK
0038                INST    EQU  X'38'      *INTERRUPT STAT.
0032                ADDM    EQU  X'32'      *ADDRESS MODE REG.
003A                ADSR    EQU  X'3A'      *ADDR. STAT. REG.
0033                AUXO    EQU  X'33'      *AUX. CMD. REG.OUT
003B                AUXI    EQU  X'3B'      *AUX. CMD. IN RE
0034                ADRG    EQU  X'34'      *ADDR. REG.
003D                SPRI    EQU  X'3D'      *SER. POL. IN.
0035                SPRO    EQU  X'35'      *SER. POL. OUT.
003C                ADSW    EQU  X'3C'      *ADDRESS SWITCH
0037                DATO    EQU  X'37'      *DATA OUT REG.
003F                DATI    EQU  X'3F'      *DATA IN REG.
2038                FBYTI   EQU  DST+32     *ADDR. 1ST BYTE.
2042                FBYTO   EQU  FBYTI+10   *488 DATA OUT.

                    ****************************************
                    *INTERRUPT HANDLER.
                    ****************************************

2038                        ORG  0
0000 31FF20                 LXI  SP,STKPT
0003 C35000                 JMP  PWRUP

0006                        ORG  X'24'      *TRAP POINTER.
0024 C30000                 JMP  0

0027                        ORG  X'34'      *INT. 6.5 POINTER.
0034 E5                     PUSH H
0035 D5                     PUSH D
0036 C5                     PUSH B
0037 F5                     PUSH PSW
0038 C3B405                 JMP  TST1

003B                        ORG  X'3C'      *INT. 7.5 POINTER.
003C E5             RST75   PUSH H
003D D5                     PUSH D
003E C5                     PUSH B
003F F5                     PUSH PSW
0040 C31302                 JMP  LEVS
```

```
                ****************************************
                *INITIALIZE ROUTINE.
                ****************************************

0043                    ORG   X'50'
0050 AF         PWRUP   XRA   A
0051 3D                 DCR   A
0052 C25100             JNZ   *-1
0055 0E09               MVI   C,9          *CLEAR 9 BYTES.
0057 AF                 XRA   A
0058 210020             LXI   H,MFLG
005B 77         NXT     MOV   M,A
005C 23                 INX   H
005D 0D                 DCR   C
005E C25B00             JNZ   NXT
0061 321520             STA   DNUM
0064 3C                 INR   A
0065 321420             STA   NSWD
0068 3ECC               MVI   A,X'CC'
006A 77                 MOV   M,A
006B 2C                 INR   L
006C 77                 MOV   M,A
006D 2C                 INR   L
006E 77                 MOV   M,A
006F 2C                 INR   L
0070 77                 MOV   M,A
0071 D300               OUT   PORT0        *INIT PORTS.
0073 3EFF               MVI   A,X'FF'
0075 D303               OUT   PORTC        *SET OUTPUTS TO 1.
0077 3EEF               MVI   A,X'EF'      *SEL. LEV, DEM1.
0079 320820             STA   DAT          *STORE 1ST DAT.
007C E6F0               ANI   X'F0'
007E D340               OUT   PORTD        *SELECT 1ST LEVEL.
0080 3EFF               MVI   A,LCNT       *COUNTER LOW BYTE.
0082 D304               OUT   PORT4
0084 3E27               MVI   A,MCNT       *COUNTER HI BYTE
0086 F6C0               ORI   X'C0'        *SET REPEAT MODE.
0088 D305               OUT   PORT5        *COUNTER PRIMED.

008A DB3C               IN    ADSW         *SETUP 488 COMM.
008C D334               OUT   ADRG
008E 3E80               MVI   A,X'80'
0090 D333               OUT   AUXO
0092 AF                 XRA   A
0093 D333               OUT   AUXO
0095 D332               OUT   ADDM
0097 DB38               IN    INST
0099 3EC1               MVI   A,X'C1'
009B D330               OUT   INTM         *ENAB. BI/BO/INT.
009D DB38               IN    INST         *CLR INT.
009F 213820             LXI   H,FBYTI
00A2 221020             SHLD  IBAS
00A5 214220             LXI   H,FBYTO
00A8 221220             SHLD  OBAS
00AB 010D00             LXI   B,13
00AE 09                 DAD   B
00AF 3620               MVI   M,' '        *'SPACE' TO 'L'.
```

```
00B1 3A0E20          LDA  MEMCK      *VERIFY MEM.VALID.
00B4 DEAA            SBI  MEMFG      *= AA HEX.
00B6 C2EA00          JNZ  ERO        *NON VALID.

                     ************************************
                     *      INITIALIZE DEMOD DATA.
                     ************************************
00B9 110800 COR1     LXI  D,8        *FORCE LOCAL.
00BC 0E04            MVI  C,TOTD
00BE CD0C02          CALL GST
00C1 3EDF    FLOC    MVI  A,X'DF'
00C3 A6              ANA  M
00C4 77              MOV  M,A
00C5 0D              DCR  C
00C6 19              DAD  D
00C7 C2C100          JNZ  FLOC
00CA 3E04    CORR    MVI  A,TOTD     *UPDATE DEMODS.
00CC 4F              MOV  C,A
00CD C5      NXTI    PUSH B          *SAVE COUNT.
00CE 320520          STA  DDEM       *NOT 0.
00D1 CDEF01          CALL TDEM
00D4 CD1803          CALL SEND       *OUT TO DEMODS.
00D7 C1              POP  B          *GET COUNT.
00D8 0D              DCR  C
00D9 CAE300          JZ   ENAB       *ALL READY.
00DC 211520          LXI  H,DNUM
00DF 34              INR  M
00E0 C3CD00          JMP  NXTI
00E3 3EC9    ENAB    MVI  A,X'C9'    *W/488 =X'49'.
00E5 30              DC   SIM        *SOD=0, 65/75 ENAB
00E6 FB              EI
00E7 C31B01          JMP  CFLG

                     ************************************
                     *      POWER UP INITIALIZE, (RAM FAIL).
                     ************************************
00EA 111820 ERO      LXI  D,DST      *1ST DEM. STAT. AD
00ED 3E04            MVI  A,TOTD
00EF 47              MOV  B,A
00F0 211001 ER1      LXI  H,INITD    *INIT. DATA.
00F3 0E08            MVI  C,8        *BYTE COUNTER
00F5 7E      ER2     MOV  A,M
00F6 12              STAX D
00F7 0D              DCR  C
00F8 CA0001          JZ   NEXD       *LAST BYTE.
00FB 23              INX  H
00FC 13              INX  D
00FD C3F500          JMP  ER2        *NEXT BYTE.
0100 05      NEXD    DCR  B          *LAST DEMOD?
0101 CA0801          JZ   OK         *YES!
0104 13              INX  D          *NO! NEXT!
0105 C3F000          JMP  ER1
                     ************************************
                     *      ALL CORRECTED.
                     ************************************
0108 3EAA    OK      MVI  A,X'AA'
```

```
010A 320E20          STA  MEMCK      *MEMORY IS VALID!
010D C3B900          JMP  COR1       *ALL DEMODS.

                *****************************************
                *1ST POWER UP DATA.
                *****************************************

0110 00      INITD   DC   00         *DEMOD VALID BYTE
0111 00              DC   00         *DEC. FREQ.= 0.
0112 00              DC   00
0113 80              DC   X'80'      *ERECT/LOC/AGC.
0114 8F              DC   X'8F'      *M. GAIN= (8F).
0115 00              DC   00
0116 00              DC   00
0117 00              DC   00
0118 02      TBAS    DC   2          *TERM.CNT. 10MSCLK
0119 10              DC   16         *   "    "  100 " "
011A 78              DC   120        *   "    "  1KC   " "
```

```
                ****************************************
                *BEGIN PANEL MONITOR.
                ****************************************

011B AF      CFLG   XRA  A
011C 320020         STA  MFLG       *CLR 1ST PASS FLAG
011F 211420  TSW    LXI  H,NSWD     *NORMAL SW. DATA.
0122 DB01           IN   PORTA      *PRESENT SW.DATA.
0124 2F             CMA             *PORT INVERTED.
0125 47             MOV  B,A
0126 3E30           MVI  A,X'30'
0128 A0             ANA  B
0129 BE             CMP  M
012A C5             PUSH B
012B C4A601         CNZ  DNO        *DEMOD SEL. CHANGE
012E C1             POP  B
012F CD0C02         CALL GST
0132 3E20           MVI  A,X'20'    *REMOTE MODE?
0134 A6             ANA  M
0135 C26E01         JNZ  RLD        *YES! NO STAT.
0138 3E03    STAT   MVI  A,3
013A A0             ANA  B
013B CA4A01         JZ   ZTF        *TUNE NOT REQ.
013E 3A0420         LDA  TNFLG
0141 B7             ORA  A
0142 C24D01         JNZ  ZTF+3
0145 3E01           MVI  A,1
0147 320220         STA  COUN
014A 320420  ZTF    STA  TNFLG      *SET FOR IMMED.
014D 3E0C           MVI  A,X'0C'
014F A0             ANA  B
0150 47             MOV  B,A
0151 CA6E01         JZ   RLD        *TEST REM/LOC SW.
0154 3A0020         LDA  MFLG
0157 B7             ORA  A
0158 C21F01         JNZ  TSW
015B 78             MOV  A,B
015C 320020         STA  MFLG       *MAKE NON ZERO.
015F 07             RLC
0160 07             RLC
0161 07             RLC
0162 07             RLC
0163 CD0C02         CALL GST
0166 AE             XRA  M          *TOGGLE CONTR BITS
0167 77             MOV  M,A        *DST CHGE
0168 CD1803         CALL SEND       *UPDATE STATI.
016B C31F01         JMP  TSW
016E AF      RLD    XRA  A
016F 320020         STA  MFLG
0172 DB3D           IN   SPRI       *TEST REM TO LOC.
0174 E640           ANI  X'40'      * REQUEST.
0176 C21F01         JNZ  TSW        *IN PROGRESS!
0179 3A0320         LDA  RMFG
017C B7             ORA  A
017D DB01           IN   PORTA      *GET R/L SWITCH.
017F C29E01         JNZ  RSW
0182 E680           ANI  X'80'
```

```
0184 CA9801          JZ   ESC
0187 CD0C02          CALL GST        *FORCE LOCAL MODE.
018A 3EDF            MVI  A,X'DF'
018C A6              ANA  M
018D 77              MOV  M,A
018E CD1803          CALL SEND
0191 3A1520          LDA  DNUM       *MERGE 'SRQ'/DNUM.
0194 F640            ORI  X'40'
0196 D335            OUT  SPRO
0198 320320 ESC      STA  RMFG
019B C31B01          JMP  CFLG
019E E680    RSW     ANI  X'80'
01A0 C21B01          JNZ  CFLG       *REQUEST MADE!
01A3 C39801          JMP  ESC        *SWITCH RELEASED.
01A6 211420 DNO      LXI  H,NSWD     *DERIVE DEM. NO.
01A9 77              MOV  M,A        * FROM SWITCH.
01AA 23              INX  H          *DNUM ADDR.
01AB 0F              RRC
01AC 0F              RRC
01AD 0F              RRC
01AE 0F              RRC
01AF 4F              MOV  C,A
01B0 3E03            MVI  A,3        *INVERSE OF SW.
01B2 91              SUB  C
01B3 77              MOV  M,A        *STORE DNUM.
01B4 CDEF01          CALL TDEM       *SET POINTER.
01B7 3C              INR  A
01B8 320520          STA  DDEM       *FLAG CHANGE.
01BB CD1803          CALL SEND       *SET ACTIVE DEM.
01BE C9              RET

01BF 210F20 RAZE     LXI  H,STSIZ
01C2 DB02            IN   PORTB      *SETUP SIZE/ RATE.
01C4 2F              CMA
01C5 4F              MOV  C,A
01C6 E603            ANI  3
01C8 CAD201          JZ   RA2        *SET =2.
01CB 1F              RAR
01CC DAD401          JC   RA2+2      *SET =1.
01CF C3D301          JMP  RA2+1      *SET =4.
01D2 37      RA2     STC
01D3 17              RAL
01D4 17              RAL
01D5 77              MOV  M,A        *STORE SIZE FLAG.
01D6 211801          LXI  H,TBAS     *DERIVE RATE.
01D9 3E0C            MVI  A,X'0C'
01DB A1              ANA  C
01DC 0F              RRC
01DD 0F              RRC
01DE 0F              RRC
01DF CAEB01          JZ   SEC+1
01E2 DAEA01          JC   SEC
01E5 7E      STOR    MOV  A,M        *STORE RATE BYTE.
01E6 320220          STA  COUN       *NEW INT. COUNTER.
01E9 C9              RET
01EA 23      SEC     INX  H          *USE TBAS+1.
01EB 23              INX  H          *USE TBAS+2.
```

```
01EC C3E501          JMP  STOR
01EF 2A1520 TDEM     LHLD DNUM       *DERIVE POINTER
01F2 2600            MVI  H,0        * FOR PRESENT DEM.
01F4 29              DAD  H          *MULT. DNUM * 8.
01F5 29              DAD  H
01F6 29              DAD  H
01F7 EB              XCHG
01F8 211820          LXI  H,DST      *ADD TO STATUS
01FB 19              DAD  D          * BASE ADDRESS.
01FC 221620          SHLD DPTR       *STORE POINTER.
01FF 23              INX  H
0200 23              INX  H
0201 23              INX  H
0202 23              INX  H
0203 23              INX  H
0204 23              INX  H
0205 3E30            MVI  A,X'30'    *EXTRACT THE PRES
0207 A6              ANA  M          * ENT BAND SWITCH.
0208 320720          STA  BAND       *SAVE IT.
020B C9              RET
020C 2A1620 GST      LHLD DPTR       *GET DEMOD STATUS
020F 23              INX  H          * ADDR. IN HL.
0210 23              INX  H
0211 23              INX  H
0212 C9              RET

                     ****************************************
                     *       ENTRY FROM INTERRUPT 7.5.      *
                     ****************************************

0213 210120 LEVS     LXI  H,TLTIM    *SERVICE LEVEL
0216 35              DCR  M          * UPDATE COUNTER.
0217 CAE603          JZ   NLEV       *SERVICE REQUIRED!
021A 23      PROC    INX  H          *SERVICE PANEL
021B 35              DCR  M          *COUNTER.
021C C21203          JNZ  ENDT       *NO SERVICE REQ.
021F CD0C02          CALL GST        *REMOTE?
0222 7E              MOV  A,M
0223 E620            ANI  X'20'
0225 C21203          JNZ  ENDT       *YES!
0228 CDBF01          CALL RAZE       *SET RATE & STEP.
022B DB01            IN   PORTA
022D 2F              CMA             *INVERT DATA.
022E 4F              MOV  C,A        *SAVE PORTA
022F E603            ANI  3          *MASK GAIN SWITCH.
0231 CAA803          JZ   MGAIN      *GAIN SW. ACTIVE.
0234 3E01            MVI  A,1        *TUNE UP?
0236 A1              ANA  C
0237 3A0F20          LDA  STSIZ
023A 4F              MOV  C,A
023B C29002          JNZ  TUNUP      *ADD TO FREQ.

023E CD0C02 TUNDN    CALL GST        *TUNE FREQ. DOWN
0241 7E              MOV  A,M        *GET MSB DEC.
0242 E6E3            ANI  X'E3'
0244 77              MOV  M,A
0245 E603            ANI  3
```

```
0247 2B            DCX  H
0248 B6            ORA  M
0249 C26302        JNZ  MIN        *3 MSB'S NOT = 0!
024C 2B            DCX  H
024D B6            ORA  M
024E CA0F03        JZ   IRET+3     *ALL= 0.
0251 79            MOV  A,C        *STSIZ TO A.
0252 E604          ANI  4
0254 C20F03        JNZ  IRET+3     *1 KC STEPS.
0257 7E            MOV  A,M        *LSB'S TO A.
0258 E6F0          ANI  X'F0'
025A C26302        JNZ  MIN        *HUND'S > 0.
025D 3E02          MVI  A,2        *STEPS= 100?
025F A1            ANA  C
0260 C20F03        JNZ  IRET+3     *YES!
0263 2A1620 MIN    LHLD DPTR     *LSB'S.
0266 23            INX  H
0267 79            MOV  A,C
0268 FE01          CPI  1
026A 0E03          MVI  C,3
026C 0601          MVI  B,1
026E CA7D02        JZ   SLOOP      *TENS!
0271 FE02          CPI  2
0273 0610          MVI  B,X'10'
0275 CA7D02        JZ   SLOOP
0278 23            INX  H
0279 0601          MVI  B,1
027B 0E02          MVI  C,2
027D 37      SLOOP STC             *SUBTRACT STPSZE.
027E 3E99          MVI  A,X'99'
0280 CE00          ACI  0
0282 90            SUB  B
0283 86            ADD  M
0284 27            DAA
0285 77            MOV  M,A
0286 0D            DCR  C
0287 CA0C03        JZ   IRET       *LAST DIGIT.
028A 0600          MVI  B,0
028C 23            INX  H
028D C37E02        JMP  SLOOP+1

0290 CD0C02 TUNUP  CALL GST        *INCREASE FREQ.
0293 7E            MOV  A,M
0294 E6E3          ANI  X'E3'
0296 77            MOV  M,A
0297 E603          ANI  3
0299 FE03          CPI  3
029B C2D602        JNZ  AD1        * MSB NOT= 3 YET!
029E 2B            DCX  H
029F 2B            DCX  H          *GET LSB'S.
02A0 7E            MOV  A,M
02A1 FE00          CPI  0
02A3 23            INX  H          *POINT TO 10-3.
02A4 CACE02        JZ   EQ8?       * LSB'S =0, KC =8?
02A7 7E            MOV  A,M        *NO, =7?
02A8 E60F          ANI  X'0F'      *SAVE THOUS.
02AA FE07          CPI  7
```

```
02AC C2D602          JNZ  AD1        *KC <7.
02AF 79              MOV  A,C        *TEST STSIZ=THOUS.
02B0 E604            ANI  4
02B2 C20F03          JNZ  IRET+3     *FREQ.=307XX.
02B5 2B              DCX  H          *LSB'S.
02B6 7E              MOV  A,M
02B7 47              MOV  B,A        *SAVE LSB'S
02B8 E60F            ANI  X'0F'
02BA 78              MOV  A,B
02BB CAD602          JZ   AD1
02BE E6F0            ANI  X'F0'      *TEST HUND'S.
02C0 FE90            CPI  X'90'
02C2 C2D602          JNZ  AD1        *HUND'S < 9.
02C5 3E02            MVI  A,2        *STSIZ=HUND'S?
02C7 B9              CMP  C
02C8 CA0F03          JZ   IRET+3     *YES!
02CB C3D602          JMP  AD1        *STSIZ=10HZ!
02CE 7E      EQ8?    MOV  A,M        KC= 8?
02CF E60F            ANI  X'0F'
02D1 FE08            CPI  8
02D3 CA0F03          JZ   IRET+3
02D6 2A1620  AD1     LHLD DPTR       *LSB'S
02D9 23              INX  H
02DA 79              MOV  A,C        *STSIZ =1?
02DB FE01            CPI  1
02DD 0E03            MVI  C,3
02DF 0601            MVI  B,1
02E1 CAF002          JZ   ALOOP-1    *YES!
02E4 FE02            CPI  2          *STSIZ =2?
02E6 0610            MVI  B,X'10'
02E8 CAF002          JZ   ALOOP-1    *YES!
02EB 23              INX  H          *THOUS. LOC.
02EC 0601            MVI  B,1
02EE 0E02            MVI  C,2
02F0 AF              XRA  A          *CLEAR CARRY.
02F1 78      ALOOP   MOV  A,B        *B = ADD BIT LOC.
02F2 8E              ADC  M
02F3 27              DAA
02F4 0D              DCR  C
02F5 CAFF02          JZ   LST
02F8 77              MOV  M,A        *STORE BYTE.
02F9 23              INX  H
02FA 0600            MVI  B,0
02FC C3F102          JMP  ALOOP
02FF 4F      LST     MOV  C,A        *SAVE STATUS DATA
0300 7E              MOV  A,M        * WITH MSB.
0301 E6F0            ANI  X'F0'
0303 47              MOV  B,A
0304 79              MOV  A,C
0305 E60F            ANI  X'0F'
0307 B0              ORA  B
0308 77              MOV  M,A
0309 C30C03          JMP  IRET
```

```
                ****************************************
                *      7.5 INT. RETURN.
                ****************************************

030C CD1803 IRET    CALL SEND       *RETURN WITH
030F CDBF01         CALL RAZE       * STATUS CHANGE.
0312 F1      ENDT   POP  PSW        *RETURN WITHOUT
0313 C1             POP  B          * STATUS CHANGE.
0314 D1             POP  D
0315 E1             POP  H
0316 FB             EI
0317 C9             RET
```

```
0318 3A0520 SEND   LDA  DDEM      *DEM CHANGED?
031B B7            ORA  A
031C CA3303        JZ   MOD       *NO!
031F 3EDF          MVI  A,X'DF'   *CLEAR 'ACTIVES'
0321 D303          OUT  PORTC
0323 E6C1          ANI  X'C1'     *ALL CLOCKS.
0325 D303          OUT  PORTC
0327 F6DF          ORI  X'DF'     *RESET CLOCKS.
0329 D303          OUT  PORTC
032B F6FF          ORI  X'FF'
032D D303          OUT  PORTC
032F AF            XRA  A
0330 320520        STA  DDEM      *DONE, CLEAR FLAG.
0333 CD0C02 MOD    CALL GST       *CONVERT 1ST L.O.
0336 7E            MOV  A,M
0337 E640          ANI  X'40'
0339 C24203        JNZ  *+9
033C CD3804        CALL ERECT
033F C34503        JMP  *+6
0342 CDAA04        CALL INVERT
0345 CD0C02        CALL GST       *SAME B.SW?
0348 23            INX  H
0349 23            INX  H
034A 23            INX  H
034B 3E30          MVI  A,X'30'
034D A6            ANA  M
034E 47            MOV  B,A
034F 3A0720        LDA  BAND
0352 B8            CMP  B
0353 2B            DCX  H
0354 78            MOV  A,B
0355 320720        STA  BAND
0358 CA6203        JZ   NCHG      *YES! SET B.SW.
035B 3E7F          MVI  A,X'7F'   * TOGGLE.
035D A6            ANA  M
035E 77            MOV  M,A
035F C36603        JMP  CLB
0362 3E80   NCHG   MVI  A,X'80'   *RESET BAND SW.
0364 B6            ORA  M         * TOGGLE.
0365 77            MOV  M,A
0366 3A1520 CLB    LDA  DNUM      *COMPUTE CLK. BIT.
0369 4F            MOV  C,A
036A 3EFE          MVI  A,X'FE'
036C 07            RLC
036D 0D            DCR  C
036E F26C03        JP   *-2
0371 47            MOV  B,A       *B=CLK BIT.
0372 2A1620        LHLD DPTR
0375 23            INX  H         *1ST BYTE.
0376 1E07          MVI  E,7       *BYTE COUNT
0378 0E08   SBIT   MVI  C,8
037A 56            MOV  D,M       *1ST BYTE.
037B 7A            MOV  A,D
037C E601   BIT    ANI  1
037E 2F            CMA
037F D303          OUT  PORTC     *DATA ONLY.
0381 CD8E03        CALL CLK       *DATA & CLK.
```

```
0384 0D            DCR  C
0385 CA9A03        JZ   NBYT      *GET NXT BYTE.
0388 7A            MOV  A,D       *NEXT BIT.
0389 1F            RAR
038A 57            MOV  D,A       *SAVE.
038B C37C03        JMP  BIT
038E A0      CLK   ANA  B         *SET CLK.= 0.
038F D303          OUT  PORTC
0391 F6FE          ORI  X'FE'     *DATA ONLY.
0393 D303          OUT  PORTC
0395 F6FF          ORI  X'FF'
0397 D303          OUT  PORTC
0399 C9            RET
039A 23      NBYT  INX  H         *NEXT
039B 1D            DCR  E
039C C27803        JNZ  SBIT
039F 3EDF          MVI  A,X'DF'   *SEND STROBE.
03A1 D303          OUT  PORTC
03A3 F6FF          ORI  X'FF'
03A5 D303          OUT  PORTC
03A7 C9            RET            *END SEND.
```

```
03A8 CD0C02 MGAIN  CALL GST        *TEST AGC MODE.
03AB 7E            MOV  A,M
03AC E680          ANI  X'80'
03AE C20F03        JNZ  IRET+3     *YES, AGC MODE!
03B1 DB02          IN   PORTB      *TEST GAIN SW.
03B3 2F            CMA
03B4 E660          ANI  X'60'
03B6 4F            MOV  C,A
03B7 CA0F03        JZ   IRET+3     *ADJUST NOT REQ.
03BA 3E20          MVI  A,' '      *CLEAR 'LIMIT'.
03BC 324F20        STA  FBYTO+13
03BF 23            INX  H          *TEST UP OR DWN.
03C0 79            MOV  A,C
03C1 E620          ANI  X'20'
03C3 C2D203        JNZ  UPTST      *GAIN UP.
03C6 3EE0          MVI  A,F4       *TEST LOWER LIMIT.
03C8 BE            CMP  M          *GAIN MIN?
03C9 CADE03        JZ   FIXR       *YES.
03CC CD7A05        CALL GDN
03CF C30C03        JMP  IRET
03D2 3E1F   UPTST  MVI  A,X'1F'    *TEST UPPER LIM.
03D4 BE            CMP  M
03D5 CADE03        JZ   FIXR       *YES!
03D8 CD3D05        CALL GUP
03DB C30C03        JMP  IRET
03DE 3E4C   FIXR   MVI  A,'L'      *SET 'L' (LIMIT)
03E0 324F20        STA  FBYTO+13   * FOR REM. CONT.
03E3 C30F03        JMP  IRET+3

                   ****************************************
                   *      ADJ. DEMOD LEVELS.              *
                   ****************************************
03E6 E5     NLEV   PUSH H          *SAVE POINTER.
03E7 3602          MVI  M,2        *RESTORE COUNTER.
03E9 DB60          IN   PORTE      *GET LEVEL.
03EB 0600          MVI  B,0
03ED 4F            MOV  C,A
03EE 3A0820        LDA  DAT        *COMPUTE LLEV
03F1 2F            CMA             * ADDRESS.
03F2 17            RAL
03F3 DAFA03        JC   *+7
03F6 04            INR  B
03F7 C3F203        JMP  *-5
03FA 210920        LXI  H,LLEV
03FD 78            MOV  A,B
03FE 85            ADD  L
03FF 6F            MOV  L,A        *HL= LLEV, THIS
0400 79            MOV  A,C        * DEMOD.
0401 BE            CMP  M
0402 CA2504        JZ   RDAT       *SAME AS LAST.
0405 77            MOV  M,A        *STORE NEW LEVEL.
0406 0E07          MVI  C,7
0408 B7            ORA  A          *TEST NEW LEVEL.
0409 CA1404        JZ   STLV-2     *LEVEL 'UNDER'
040C 1F     RINC   RAR             *GET BCD IN C.
040D DA1604        JC   STLV
0410 0D            DCR  C
```

```
0411 C30C04          JMP   RINC
0414 0E08            MVI   C,8        *LEVEL 'UNDER'
0416 210820 STLV     LXI   H,DAT
0419 7E              MOV   A,M
041A E6F0            ANI   X'F0'      *KILL LSN.
041C B1              ORA   C          *MERGE ADDR/LEVEL.
041D D340            OUT   PORTD
041F 3E40            MVI   A,X'40'    *0 TO SOD.(CLOCK)
0421 30              DC    SIM
0422 F6C0            ORI   X'C0'
0424 30              DC    SIM
0425 210820 RDAT     LXI   H,DAT      *DAT= 7F HEX?
0428 7E              MOV   A,M
0429 07              RLC
042A DA2F04          JC    *+5        *NO!
042D 3EEF            MVI   A,X'EF'    *YES! RESTORE.
042F 77              MOV   M,A
0430 E6F0            ANI   X'F0'
0432 D340            OUT   PORTD      *SET LEV. ADDR.
0434 E1              POP   H
0435 C31A02          JMP   PROC
                     ***********************************
                     *ERECT, 1ST L.O. CONVERSION.
                     ***********************************

0438 2A1620 ERECT    LHLD  DPTR
043B 23              INX   H
043C 7E              MOV   A,M        *GET LSB'S DEC.
043D E5              PUSH  H          *SAVE ADDRESS.
043E CD8C04          CALL  BCDBN      *CONV. TO BINARY.
0441 45              MOV   B,L        *PARTIAL TO B.
0442 E1              POP   H
0443 23              INX   H
0444 E5              PUSH  H          *SAVE 2ND ADDR.
0445 23              INX   H
0446 23              INX   H
0447 23              INX   H
0448 70              MOV   M,B        *STORE F(AB)
0449 EB              XCHG             *LO1 ADDR TO DE.
044A E1              POP   H          *2ND LSB TO HL.
044B 7E              MOV   A,M
044C E60F            ANI   X'0F'      *SAVE LSB DEC.
044E EB              XCHG
044F 23              INX   H          *LO2 ADDR.
0450 77              MOV   M,A        *3 MSB'S OF LOF.
0451 EB              XCHG
0452 7E              MOV   A,M        *10-3 TO A.
0453 E6F0            ANI   X'F0'      *SAVE MSB.
0455 47              MOV   B,A        *SAVE  "
0456 23              INX   H
0457 7E              MOV   A,M        *10-5 TO A.
0458 E603            ANI   3          *< 3.
045A B0              ORA   B          *MERGE.
045B 07              RLC
045C 07              RLC
045D 07              RLC
045E 07              RLC
```

```
045F D5              PUSH D          *SAVE LO2 ADDR.
0460 CD8C04          CALL BCDBN      *CONV 10-4,10-5.
0463 3EDB            MVI  A,X'DB'    *CONSTANT OFFSET.
0465 95              SUB  L          *A= LO3
0466 E1              POP  H          *WAS IN DE.
0467 23              INX  H          *LO3 ADDR.
0468 77              MOV  M,A        *STORE LOC, A & B.
0469 0603            MVI  B,3        *SET BAND SW.
046B FED2            CPI  X'D2'      *B.SW.=3?
046D D27D04          JNC  STRB       *YES!
0470 05              DCR  B
0471 FEC3            CPI  X'C3'
0473 D27D04          JNC  STRB
0476 05              DCR  B
0477 FEB4            CPI  X'B4'
0479 D27D04          JNC  STRB
047C 05              DCR  B          *B=0!
047D 2B      STRB    DCX  H
047E 78              MOV  A,B        *JUSTIFY B.SW.
047F 07              RLC
0480 07              RLC
0481 07              RLC
0482 07              RLC
0483 47              MOV  B,A
0484 3E0F            MVI  A,X'0F'
0486 A6              ANA  M          *KEEP LOF BITS.
0487 F640            ORI  X'40'      *SET LOC, C =1.
0489 B0              ORA  B          *SET BAND SW. BITS
048A 77              MOV  M,A        *RESTORE BYTE.
048B C9              RET
048C 110A00  BCDBN   LXI  D,X'000A'  *BCD TO BINARY.
048F 210000          LXI  H,0        *2 DIG. BCD IN A.
0492 6F              MOV  L,A
0493 29              DAD  H
0494 29              DAD  H
0495 29              DAD  H
0496 29              DAD  H
0497 44              MOV  B,H
0498 E60F            ANI  X'0F'
049A 4F              MOV  C,A
049B 210000          LXI  H,0
049E 04              INR  B
049F 05      NX      DCR  B
04A0 CAA704          JZ   ADL
04A3 19              DAD  D
04A4 C39F04          JMP  NX
04A7 09      ADL     DAD  B
04A8 7D              MOV  A,L
04A9 C9              RET

                     ************************************
                     *INVERT, 1ST LO CONVERSION.
                     ************************************

04AA 2A1620  INVERT  LHLD DPTR
04AD 23              INX  H          *H=D1A(DEC. 1 ADDR
04AE AF              XRA  A
```

```
04AF BE            CMP  M          *LSB = 0?
04B0 E5            PUSH H
04B1 D1            POP  D
04B2 010400        LXI  B,4
04B5 09            DAD  B
04B6 CAC404        JZ   STO        *YES!
04B9 1A            LDAX D
04BA D5            PUSH D
04BB E5            PUSH H
04BC CD8C04        CALL BCDBN      *NO! CONVERT!
04BF 3E64          MVI  A,100      *COMPLIMENT IT!
04C1 95            SUB  L
04C2 E1            POP  H
04C3 D1            POP  D
04C4 77      STO   MOV  M,A        *STORE FA & FB.
04C5 320D20        STA  F0         *SET FLAG.
04C8 EB            XCHG            *H=D1;D=F1.
04C9 4E            MOV  C,M
04CA 23            INX  H          *H= 2ND & 3RD LSB.
04CB E5            PUSH H
04CC 7E            MOV  A,M
04CD E60F          ANI  X'0F'
04CF 47            MOV  B,A
04D0 21AFFC        LXI  H,X'FCAF'  *COMPL. OF 350.
04D3 09            DAD  B
04D4 EB            XCHG            *H= F1.
04D5 D1            POP  D          *D= D2.
04D6 F5            PUSH PSW        *SAVE '3.50' STAT.
04D7 E5            PUSH H          *SAVE 2ND LO ADDR.
04D8 1A            LDAX D
04D9 6F            MOV  L,A        *2 MSB'S DEC. TO
04DA 13            INX  D          *HL REGISTER.
04DB 1A            LDAX D
04DC 67            MOV  H,A        *MSB TO H.
04DD 29            DAD  H
04DE 29            DAD  H
04DF 29            DAD  H
04E0 29            DAD  H          *SWAP NIBBLES.
04E1 7C            MOV  A,H
04E2 D5            PUSH D
04E3 CD8C04        CALL BCDBN      *GET BINARY EQUIV.
04E6 D1            POP  D
04E7 4D            MOV  C,L        *SAVE CONV.
04E8 E1            POP  H          *H= F1.
04E9 23            INX  H
04EA 23            INX  H          *H= F3.
04EB F1            POP  PSW
04EC F5            PUSH PSW        *CY=1;>350.
04ED 79            MOV  A,C
04EE CEE1          ACI  X'E1'      *ADD OFFSET & CY.
04F0 77            MOV  M,A        *STORE CA & CB.
04F1 3E00          MVI  A,0
04F3 CE01          ACI  1
04F5 2B            DCX  H          *H= LO 2ND BYTE.
04F6 0F            RRC
04F7 0F            RRC
04F8 77            MOV  M,A        *STORE CC.
```

```
04F9 FE40          CPI  X'40'     *TEST BAND SWITCH.
04FB C20B05        JNZ  TWO       *B. SW. =2!
04FE 23            INX  H         *H= 3RD LO BYTE.
04FF 3EF3          MVI  A,X'F3'
0501 BE            CMP  M
0502 2B            DCX  H
0503 DA0B05        JC   TWO
0506 3E10          MVI  A,X'10'   *BAND SWITCH = 1.
0508 C30D05        JMP  TWO+2
050B 3E20   TWO    MVI  A,X'20'   *  "    "    = 2.
050D B6            ORA  M
050E 77            MOV  M,A
050F EB            XCHG           *D= 2ND LO BYTE.
0510 CD0C02        CALL GST
0513 2B            DCX  H
0514 3E0F          MVI  A,X'0F'   *GET 3RD DEC. DIG.
0516 A6            ANA  M
0517 47            MOV  B,A
0518 F1            POP  PSW
0519 DA2A05        JC   ELEV
051C 3E07          MVI  A,7
051E 90            SUB  B
051F 47            MOV  B,A
0520 2B            DCX  H
0521 AF            XRA  A
0522 BE            CMP  M
0523 C23605        JNZ  NZRO
0526 04            INR  B
0527 C33605        JMP  NZRO
052A 3E11   ELEV   MVI  A,X'11'
052C 90            SUB  B
052D 47            MOV  B,A
052E 3A0D20        LDA  F0
0531 B7            ORA  A
0532 C23605        JNZ  NZRO
0535 04            INR  B
0536 EB     NZRO   XCHG
0537 3EF0          MVI  A,X'F0'
0539 A6            ANA  M
053A B0            ORA  B
053B 77            MOV  M,A
053C C9            RET

           ************************************
           *      GAIN ADJUST UP ROUTINE.     *
           ************************************
053D 7E     GUP    MOV  A,M       *HL= GAIN BYTE.
053E 4F            MOV  C,A
053F E61F          ANI  X'1F'     *KILL ATTEN.
0541 FE16          CPI  UL        *ADC = UL?
0543 CA4E05        JZ   MING      *YES; PAD MAX?
0546 47            MOV  B,A       *NO; INCR ADC.
0547 04     LAST   INR  B
0548 3EE0          MVI  A,X'E0'
054A A1            ANA  C
054B B0            ORA  B
054C 77            MOV  M,A       *STORE NEW GAIN.
```

```
054D C9              RET
054E 79      MING    MOV   A,C
054F E6E0            ANI   X'E0'      *KILL ADC.
0551 B7              ORA   A
0552 C25C05          JNZ   MIN1
0555 79              MOV   A,C
0556 E61F            ANI   X'1F'
0558 47              MOV   B,A
0559 C34705          JMP   LAST
055C FEE0    MIN1    CPI   P4         ATTEN MAX?
055E CA7405          JZ    NP3        *DECREASE PAD.
0561 FEC0            CPI   P3
0563 CA7105          JZ    NP2
0566 FE60            CPI   P2
0568 CA6E05          JZ    NP1
056B 360D            MVI   M,LL       *MUST BE 1.
056D C9              RET
056E 362D    NP1     MVI   M,P1+LL
0570 C9              RET
0571 366D    NP2     MVI   M,P2+LL
0573 C9              RET
0574 36CD    NP3     MVI   M,P3+LL
0576 C9              RET
0577 36ED    NP4     MVI   M,P4+LL
0579 C9              RET

             ************************************
             *       GAIN DOWN ADJUST ROUTINE.
             ************************************
057A 7E      GDN     MOV   A,M        *HL= GAIN BYTE.
057B 4F              MOV   C,A
057C E61F            ANI   X'1F'      *EXTRACT COUNTER.
057E FE0D            CPI   LL         *LOWER LIMIT?
0580 CA8B05          JZ    PAD        *YES!
0583 3D      GUP1    DCR   A
0584 47              MOV   B,A        *SAVE DEC. COUNT.
0585 3EE0            MVI   A,X'E0'    *EXTRACT PADS.
0587 A1              ANA   C
0588 B0              ORA   B          *MERGE BOTH.
0589 77              MOV   M,A        *STORE NEW GAIN.
058A C9              RET
058B 3EE0    PAD     MVI   A,X'E0'    *SET NEXT PAD.
058D A1              ANA   C
058E FEE0            CPI   P4         *ALL PADS IN?
0590 CAAE05          JZ    GZRO       *YES!
0593 FEC0            CPI   P3
0595 CAAB05          JZ    PP4
0598 FE60            CPI   P2         *ATTEN = 6DB?
059A CAA805          JZ    PP3        *YES!
059D FE20            CPI   P1         *12?
059F CAA505          JZ    PP2
05A2 3636            MVI   M,P1+UL
05A4 C9              RET
05A5 3676    PP2     MVI   M,P2+UL
05A7 C9              RET
05A8 36D6    PP3     MVI   M,P3+UL
05AA C9              RET
```

```
05AB 36F6   PP4     MVI   M,P4+UL
05AD C9             RET
05AE 3E1F   GZRO    MVI   A,X'1F'    *NO PADS NOW!
05B0 A1             ANA   C
05B1 C38305         JMP   GUP1


                    ************************************
                    *       BTALK- BASIC TALKER, 8080.
                    *       BLIST-   "   LISTENER  "
                    ************************************

05B4 DB3A   TST1    IN    ADSR        *LISTENER?
05B6 FE86           CPI   X'86'
05B8 CAE905         JZ    LINT        *YES!
05BB FE89           CPI   X'89'       *TALKER?
05BD C21203         JNZ   ENDT        *NO! GET OUT.

                    ************************************
                    *        BTALK.
                    ************************************

05C0 DB38           IN    INST        *RESET INTERRUPT.
05C2 E640           ANI   X'40'
05C4 CAC005         JZ    *-4
05C7 AF             XRA   A
05C8 D335           OUT   SPRO        *CLEAR SERV. REQ.
05CA 2A1220 BTALK   LHLD  OBAS        *GET DATA ADDR.
05CD 7E             MOV   A,M
05CE D337           OUT   DATO        *OUTPUT DATA BYTE.
05D0 23             INX   H
05D1 221220         SHLD  OBAS        *STORE POINTER.
05D4 FE0A           CPI   X'0A'       *LAST CHARACTER?
05D6 C21203         JNZ   ENDT        *NO!
05D9 214220 LBYT    LXI   H,FBYTO     *YES! RESET PNTR.
05DC 221220         SHLD  OBAS
05DF DB38           IN    INST        *CLEAR LAST INT.
05E1 E640           ANI   X'40'
05E3 CADF05         JZ    *-4
05E6 C31203         JMP   ENDT        *BACK TO PANEL.

                    ****************************************
                    *        BLIST- BASIC LISTENER-8080.
                    ****************************************

05E9 2A1020 LINT    LHLD  IBAS        *SET POINTER.
05EC DB38   IDAT    IN    INST        *CLEAR INTERRUPT.
05EE E601           ANI   1
05F0 CAEC05         JZ    IDAT
05F3 DB3F           IN    DATI        *GET DATA.
05F5 77             MOV   M,A         *1ST BYTE IN, ETC.
05F6 23             INX   H
05F7 221020         SHLD  IBAS        *REPLACE POINTER.
05FA FE0A           CPI   X'0A'       *LAST CHARACTER?
05FC C21203         JNZ   ENDT
                    ************************************
                    *       SETUP DATA FOR 488 OUT.
```

```
                ************************************
05FF 213820 JTBLT   LXI  H,FBYTI   *REPLACE POINTER.
0602 221020         SHLD IBAS
0605 113820         LXI  D,FBYTI
0608 7E             MOV  A,M
0609 FE44           CPI  'D'       *1ST BYTE= 'D'?
060B CA6306         JZ   DEMN      *YES!
060E 3A0620         LDA  RDNUM     *NO! SETUP FOR
0611 321520         STA  DNUM      * REMOTE DEMOD.
0614 CDEF01         CALL TDEM
0617 CD0C02         CALL GST       *IN REMOTE MODE?
061A 7E             MOV  A,M
061B E620           ANI  X'20'
061D 113820         LXI D,FBYTI
0620 C22906         JNZ  REMT      *YES!
0623 1A             LDAX D         *1ST BYTE = 'R'?
0624 FE52           CPI  'R'
0626 C2A006         JNZ  LOC       *NOT REMOTE REQ.
0629 214706 REMT    LXI  H,CHT     *MATCH CHARACTER.
062C 0607           MVI  B,JTBL-CHT
062E 0E00           MVI  C,0
0630 1A             LDAX D
0631 BE      LP1    CMP  M
0632 CA3E06         JZ   CJT       *CHAR. MATCH.
0635 05             DCR  B         *NO MATCH YET!
0636 CA1203         JZ   ENDT      *END OF TABLE.
0639 0C             INR  C         *NOT E.O.T.
063A 23             INX  H         *GET NEXT CHAR.
063B C33106         JMP  LP1
063E 214E06 CJT     LXI  H,JTBL
0641 79             MOV  A,C
0642 07             RLC            *(*2)
0643 81             ADD  C         *(*3)
0644 85             ADD  L         *ADD TO JTBL BASE.
0645 6F             MOV  L,A
0646 E9             PCHL           *JUMP TO ROUTINE.
0647 4C      CHT    DC   'L'
0648 52             DC   'R'       *REMOTE.
0649 41             DC   'A'       *AGC/MAN CHGE.
064A 47             DC   'G'       *GAIN CHGE.
064B 49             DC   'I'       *ERECT/INV. CHGE.
064C 45             DC   'E'
064D 46             DC   'F'       *FREQUENCY UPDATE.
064E C3A006 JTBL    JMP  LOC       *JUMP TABLE.
0651 C3AA06         JMP  RE
0654 C39106         JMP  AGC
0657 C3B206         JMP  MG
065A C3E606         JMP  IN
065D C3EE06         JMP  ERE
0660 C3F806         JMP  FRQ
0663 13      DEMN   INX  D         *SETUP DEMOD NO.
0664 EB             XCHG           *H= D NUMBER.
0665 3E03           MVI  A,3
0667 A6             ANA  M         *GET DEMOD NO.
0668 320620         STA  RDNUM
066B 211520         LXI  H,DNUM
066E BE             CMP  M
```

```
066F 321520          STA  DNUM
0672 CA1E07          JZ   ASCII      *SAME DEMOD.
0675 2B              DCX  H          *NSWD ADDR.
0676 3C              INR  A
0677 77              MOV  M,A
0678 C31E07          JMP  ASCII
067B 3A0620 RCMD     LDA  RDNUM
067E 211520          LXI  H,DNUM
0681 77              MOV  M,A
0682 2B              DCX  H
0683 3C              INR  A
0684 77              MOV  M,A
0685 320520          STA  DDEM       *FLAG DEM. CHANGE.
0688 CDEF01          CALL TDEM
068B CD1803          CALL SEND       *UPDATE DEMOD.
068E C31E07          JMP  ASCII
0691 CD0C02 AGC      CALL GST        *SET AGC/MAN BIT.
0694 3E80            MVI  A,X'80'
0696 B6              ORA  M
0697 77              MOV  M,A
0698 214F20          LXI  H,FBYTO+13
069B 3620            MVI  M,' '      *'SPACE' TO 'L'.
069D C37B06          JMP  RCMD
06A0 CD0C02 LOC      CALL GST        *0 TO LOC/REM BIT.
06A3 3EDF            MVI  A,X'DF'
06A5 A6              ANA  M
06A6 77              MOV  M,A
06A7 C37B06          JMP  RCMD
06AA CD0C02 RE       CALL GST        *1 TO LOC/REM BIT.
06AD 3E20            MVI  A,X'20'
06AF C39606          JMP  AGC+5
06B2 CD0C02 MG       CALL GST        *0 TO MAN/AGC BIT.
06B5 3E7F            MVI  A,X'7F'
06B7 A6              ANA  M
06B8 77              MOV  M,A
06B9 23              INX  H          *GAIN BYTE.
06BA 13              INX  D          *+/- BYTE.
06BB 1A              LDAX D
06BC FE2B            CPI  X'2B'      *'+'?
06BE 114F20          LXI  D,FBYTO+13
06C1 3E20            MVI  A,' '      *'SPACE' TO 'L'.
06C3 12              STAX D
06C4 CACA06          JZ   *+6        *YES!
06C7 C3D606          JMP  DN
06CA 3E1F            MVI  A,X'1F'
06CC BE              CMP  M          *UP LIMIT?
06CD CCE206          CZ   LIM        *YES!
06D0 C43D05          CNZ  GUP
06D3 C37B06          JMP  RCMD
06D6 3EE0    DN      MVI  A,X'E0'
06D8 BE              CMP  M          *LOW LIMIT?
06D9 CCE206          CZ   LIM        *YES!
06DC C47A05          CNZ  GDN
06DF C37B06          JMP  RCMD
06E2 3E4C    LIM     MVI  A,'L'      *AT LIMIT.
06E4 12              STAX D
06E5 C9              RET
```

```
06E6 CD0C02 IN      CALL GST        *MAKE INVERT.
06E9 3E40           MVI  A,X'40'
06EB C39606         JMP  AGC+5
06EE CD0C02 ERE     CALL GST        *MAKE ERECT.
06F1 3EBF           MVI  A,X'BF'
06F3 A6             ANA  M
06F4 77             MOV  M,A
06F5 C37B06         JMP  RCMD
06F8 CD0C02 FRQ     CALL GST        *UPDATE FREQUENCY.
06FB 0E02           MVI  C,2        *COUNTER.
06FD 13             INX  D          *POINT TO MSB, ASC
06FE 1A             LDAX D          *GET BYTE, ASCII.
06FF E60F           ANI  X'0F'      *KILL ASCII.
0701 47             MOV  B,A
0702 3EF0           MVI  A,X'F0'
0704 A6             ANA  M
0705 B0             ORA  B          *MERGE MSD/STATUS.
0706 77             MOV  M,A        *STORE IT.
0707 13      FR2    INX  D          *NEXT ASCII INPUT.
0708 2B             DCX  H          *2ND LSB'S DEC.
0709 1A             LDAX D
070A E60F           ANI  X'0F'      *KILL ASCII.
070C 07             RLC
070D 07             RLC
070E 07             RLC
070F 07             RLC
0710 47             MOV  B,A
0711 13             INX  D
0712 1A             LDAX D
0713 E60F           ANI  X'0F'
0715 B0             ORA  B
0716 77             MOV  M,A
0717 0D             DCR  C
0718 C20707         JNZ  FR2        *LOOP TWICE.
071B C37B06         JMP  RCMD

                    ****************************************
                    *       ASCII CONVERSION, STORE
                    *         DATA FOR BASIC TALKER.
                    ****************************************
071E 214220 ASCII   LXI  H,FBYTO    *1ST BYTE OUT
0721 3644           MVI  M,'D'      * IS A 'D'.
0723 23             INX  H
0724 3A0620         LDA  RDNUM      *INSERT DEM. NO.
0727 F630           ORI  X'30'      *MAKE ASCII.
0729 77             MOV  M,A        *NUMBER STORED.
072A 23             INX  H
072B E5             PUSH H
072C CDEF01         CALL TDEM
072F CD0C02         CALL GST
0732 7E             MOV  A,M        *GET STATUS GROUP.
0733 E6E0           ANI  X'E0'
0735 17             RAL             *TEST AGC/MAN.
0736 E1             POP  H
0737 DA3F07         JC   AG         *AGC MODE.
073A 364D           MVI  M,'M'      *MANUAL MODE.
073C C34107         JMP  AG+2
```

```
073F 3641    AG     MVI  M,'A'      *AGC MODE.
0741 23             INX  H          *GET ER/INV. BYTE.
0742 17             RAL
0743 DA4B07         JC   NER        *NOT ERECT.
0746 3645           MVI  M,'E'      *SET ERECT.
0748 C34D07         JMP  NER+2
074B 3649    NER    MVI  M,'I'      *SET INVERT.
074D 23             INX  H
074E 17             RAL
074F DA5707         JC   RT
0752 364C           MVI  M,'L'      *SET LOC.
0754 C35907         JMP  RT+2
0757 3652 .  RT     MVI  M,'R'      *SET REMOTE.
0759 23             INX  H
075A 3646           MVI  M,'F'      *ADD FREQ. SIGN.
075C 23             INX  H
075D EB             XCHG
075E CD0C02         CALL GST        *GET FREQ, ASCII.
0761 0E02           MVI  C,2
0763 3E0F           MVI  A,X'0F'
0765 A6             ANA  M
0766 F630           ORI  X'30'
0768 12             STAX D          *MSD STORE.
0769 13             INX  D
076A 2B             DCX  H
076B 3EF0    FRQ1   MVI  A,X'F0'
076D A6             ANA  M
076E 0F             RRC
076F 0F             RRC
0770 0F             RRC
0771 0F             RRC
0772 F630           ORI  X'30'
0774 12             STAX D
0775 13             INX  D
0776 3E0F           MVI  A,X'0F'
0778 A6             ANA  M
0779 F630           ORI  X'30'
077B 12             STAX D
077C 13             INX  D
077D 0D             DCR  C
077E 2B             DCX  H
077F C26B07         JNZ  FRQ1       *2 PASSES FOR LSD.
0782 EB             XCHG
0783 3656           MVI  M,'V'      *ADD LEVEL SIGN.
0785 23             INX  H
0786 3A0620         LDA  RDNUM      *SET DEM. LEVEL
0789 3C             INR  A          * ADDRESS LINE.
078A 4F             MOV  C,A
078B 3EEF           MVI  A,X'EF'
078D 0D      CAL    DCR  C
078E CA9507         JZ   MSK
0791 07             RLC
0792 C38D07         JMP  CAL
0795 E6F0    MSK    ANI  X'F0'
0797 D340           OUT  PORTD      *ADDRESS SET.
0799 0D             DCR  C          *WAIT.
079A C29907         JNZ  *-1
```

```
079D DB60          IN   PORTE     *GET LEVEL.
079F 47            MOV  B,A
07A0 3A0820        LDA  DAT
07A3 E6F0          ANI  X'F0'
07A5 D340          OUT  PORTD     *REPLACE ADDRESS.
07A7 78            MOV  A,B
07A8 0E07          MVI  C,7       *COMPUTE LEVEL IN
07AA B7            ORA  A         * DECIMAL.
07AB CAB607        JZ   UND
07AE 1F      RONC  RAR
07AF DABB07        JC   UND+5
07B2 0D            DCR  C
07B3 C3AE07        JMP  RONC
07B6 3655    UND   MVI  M,'U'     *'U' FOR UNDER.
07B8 C3C607        JMP  INH
07BB 3E08          MVI  A,8
07BD 91            SUB  C
07BE FE01          CPI  1
07C0 CAD007        JZ   OVR
07C3 F630          ORI  X'30'     =MAKE ASCII.
07C5 77            MOV  M,A
07C6 23      INH   INX  H
07C7 23            INX  H         *SKIP GAIN BYTE.
07C8 360D          MVI  M,X'0D'   *CARRIAGE RETURN.
07CA 23            INX  H
07CB 360A          MVI  M,X'0A'   *LINE FEED.
07CD C31203        JMP  ENDT
07D0 364F    OVR   MVI  M,'O'     *'O' FOR OVER.
07D2 C3C607        JMP  INH
07D5               END  0
```

B	0000	C	0001	D	0002	E	0003
H	0004	L	0005	M	0006	A	0007
SP	0006	PSW	0006	MFLG	2000	TLTIM	2001
COUN	2002	RMFG	2003	TNFLG	2004	DDEM	2005
RDNUM	2006	BAND	2007	DAT	2008	LLEV	2009
FO	200D	MEMCK	200E	STSIZ	200F	IBAS	2010
OBAS	2012	NSWD	2014	DNUM	2015	DPTR	2016
DST	2018	MEMFG	00AA	PORTO	0000	PORTA	0001
PORTB	0002	PORTC	0003	PORTD	0040	PORTE	0060
PORT4	0004	PORT5	0005	STKPT	20FF	LCNT	00FF
MCNT	0027	TOTD	0004	SIM	0030	RIM	0020
P4	00E0	P3	00C0	P2	0060	P1	0020
UL	0016	LL	000D	INTM	0030	INST	0038
ADDM	0032	ADSR	003A	AUXO	0033	AUXI	003B
ADRG	0034	SPRI	003D	SPRO	0035	ADSW	003C
DATO	0037	DATI	003F	FBYTI	2038	FBYTO	2042
RST75	003C	PWRUP	0050	NXT	005B	COR1	00B9
FLOC	00C1	CORR	00CA	NXTI	00CD	ENAB	00E3
ERO	00EA	ER1	00F0	ER2	00F5	NEXD	0100
OK	0108	INITD	0110	TBAS	0118	CFLG	011B
TSW	011F	STAT	0138	ZTF	014A	RLD	016E
ESC	0198	RSW	019E	DNO	01A6	RAZE	01BF
RA2	01D2	STOR	01E5	SEC	01EA	TDEM	01EF
GST	020C	LEVS	0213	PROC	021A	TUNDN	023E
MIN	0263	SLOOP	027D	TUNUP	0290	EQ8?	02CE
AD1	02D6	ALOOP	02F1	LST	02FF	IRET	030C
ENDT	0312	SEND	0318	MOD	0333	NCHG	0362
CLB	0366	SBIT	0378	BIT	037C	CLK	038E
NBYT	039A	MGAIN	03A8	UPTST	03D2	FIXR	03DE
NLEV	03E6	RINC	040C	STLV	0416	RDAT	0425
ERECT	0438	STRB	047D	BCDBN	048C	NX	049F
ADL	04A7	INVERT	04AA	STO	04C4	TWO	050B
ELEV	052A	NZRO	0536	GUP	053D	LAST	0547
MING	054E	MIN1	055C	NP1	056E	NP2	0571
NP3	0574	NP4	0577	GDN	057A	GUP1	0583
PAD	058B	PP2	05A5	PP3	05A8	PP4	05AB
GZRO	05AE	TST1	05B4	BTALK	05CA	LBYT	05D9
LINT	05E9	IDAT	05EC	JTBLT	05FF	REMT	0629
LP1	0631	CJT	063E	CHT	0647	JTBL	064E
DEMN	0663	RCMD	067B	AGC	0691	LOC	06A0
RE	06AA	MG	06B2	DN	06D6	LIM	06E2
IN	06E6	ERE	06EE	FRQ	06F8	FR2	0707
ASCII	071E	AG	073F	NER	074B	RT	0757
FRQ1	076B	CAL	078D	MSK	0795	RONC	07AE
UND	07B6	INH	07C6	OVR	07D0		

5.3.4.6 Test Points and Variable Components

Table 5-18 lists the Demodulator test points and variable components along with their nominal values, or the paragraph reference to their adjustment procedures.

Table 5-18. Test Points and Variable Components

Assembly	Figure Number	Test Point	Component	Read/Refer To
A1	7-4	TP1		+5.0 ±0.25 Vdc
		TP2		+5.0 ±0.25 Vdc
		TP3		+15.0 ±0.50 Vdc
		TP4		Gnd.
		TP5		-15.0 ±0.50 Vdc
		TP6		+4.0 Vdc Unregulated
A1A1A1/ A1A1A2	7-3		R58	Paragraph 5.3.4.7
A2A1A2	7-10		R10	Paragraph 5.3.4.7
A3A1	7-13		R22	Paragraph 5.3.4.7
A3A1A1	7-14	TP1		Note 1
		TP2		Note 1
			C16	Paragraph 5.3.4.7
			T1	Note 2
A3A1A2	7-15	TP1		Note 1
		TP2		Note 1
			C12	Paragraph 5.3.4.7
			T1	Note 2
A3A1A3	7-16	TP1		Note 1
		TP2		Note 1
			C16	Paragraph 5.3.4.7
			T1	Note 2
A3A1A4	7-17		R37	12.3 Ω (in-circuit, nominal)
A3A1A5	7-18		R2	1.51 kΩ (in-circuit, nominal)
A3A1A6	7-19	TP1		Note 3
			R16	Note 3
			R45	Paragraph 5.3.4.7

Notes:

1. Variable dc voltage dependent upon selected frequency; voltage range from -6.0 Vdc to +7.0 Vdc.
2. T1 - factory adjustable only, potted component.
3. 2 MHz carrier. Use spectrum analyzer with short leads to TP and nearest ground. R16 nominally set for mid-range; adjust for null.

5.3.4.7 Adjustment/Alignment Procedures

The following adjustment and alignment procedures should not be performed on a routine basis, but instead be used as aids in troubleshooting and/or post-repair adjustment or alignment. Prior to performing any alignment or adjustment procedure contained in this paragraph, ensure that said alignment or adjustment is absolutely necessary.

5.3.4.7.1 Manual and Automatic Gain Levels and Control

1. Remove protective covers from control unit and demodulator unit to be adjusted and connect to control rack frame via extenders/test adapters.

2. Connect test equipment to the Demodulator as shown in Figure 5-6.

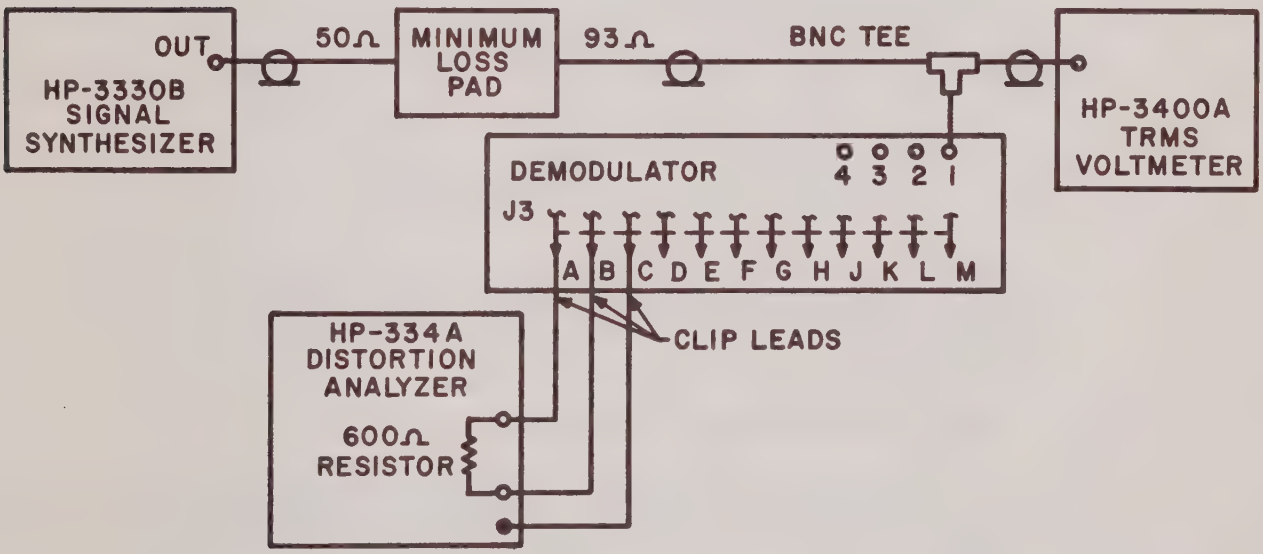


Figure 5-6. Adjustment Setup, Manual and Automatic Gain Levels and Control

3. Set Demodulator as follows:

a.	POWER	-	Off
b.	Rear Panel Routing Switches	-	BRDG position
c.	Phone LEVEL	-	Max. CCW
d.	DEMODULATOR SELECT	-	1

4. Set Demodulator POWER switch to ON position, demodulator unit to LOCAL, 000.00 kHz, ERECT, and in MANUAL gain mode.

5. Set signal synthesizer output frequency to provide 1 kHz and output level of 1.71 mV as indicated on TRMS voltmeter.

6. Adjust resistor R22 on demodulator unit motherboard to mid range position.

7. Using control unit INCR/DECR switch, adjust demodulator unit gain to maximum gain as indicated on demodulator unit dBm OVER UNDER level indicators.

NOTE

The outputs from AUDIO OUTPUT connector J3 are grouped as follows:

1 - A, B, and C (gnd)
2 - D, E, and F (gnd)
3 - G, H, and J (gnd)
4 - K, L, and M (gnd)

8. While observing distortion analyzer, adjust resistor R37 on demodulator unit input converter assembly A1A4 for output level of -5 dBm ±1 dBm and record output level.

NOTE

After performing the following step, step 9, when aligning the first demodulator unit, do not perform step 9 when aligning any other demodulator units associated with the control unit.

9. While observing demodulator dBm OVER UNDER level indicators, adjust resistor R10 on control unit panel interface and demodulator control assembly A2A1A2 for -5 dBm as indicated on demodulator unit.

10. Using INCR/DECR switch, adjust gain for minimum gain.

11. While observing distortion analyzer, increase signal synthesizer output level until audio output level is -5 dBm ±1 dBm. The signal synthesizer output level change indicated on the TRMS voltmeter is at least 40 dBm from the level indicated in step 7.

12. While observing TRMS voltmeter, adjust signal synthesizer output level to 1.71 mV.

13. Using control unit AGC/MAN switch, set demodulator unit for AGC mode.

14. While observing distortion analyzer, adjust resistor R45 on demodulator unit IF demodulator assembly A1A6 for output level of -5 dBm ±1 dBm.

15. While observing distortion analyzer, adjust signal synthesizer output to provide an output level of 0.171 V as indicated on TRMS voltmeter. The observed audio output change does not exceed 3 dBm.

16. Disconnect clip leads from connector J3 and measuring leads from distortion analyzer.

17. Remove 600 Ω resistor from distortion analyzer input.

18. Connect coax measuring lead to Demodulator connector J5 and to distortion analyzer (terminated in 93 Ω, voltmeter mode).

19. While observing distortion analyzer, adjust resistor R58 on control rack frame baseband distribution amplifier assembly A1A1A1 for 0.171 V as indicated on distortion analyzer.

20. Disconnect coax measuring lead from Demodulator connector J5 and connect to connector J6.

21. While observing distortion analyzer, adjust resistor R58 on control rack frame baseband distribution amplifier assembly A1A1A2 for 0.171 V as indicated on distortion analyzer.

22. Set Demodulator POWER switch to off position; remove demodulator unit from extender/test adapter; reinstall demodulator unit protective cover; and reinstall demodulator unit in Demodulator.

23. Repeat steps 1 through 8 and 10 through 15 for remaining demodulator units which require adjustment/alignment.

5.3.4.7.2 Tuning Voltages, Resolution, Range, and Accuracy

1. Remove protective cover from demodulator unit to be adjusted and connect to control rack frame via extender/test adapter.

2. Connect test equipment to the Demodulator as shown in Figure 5-7.

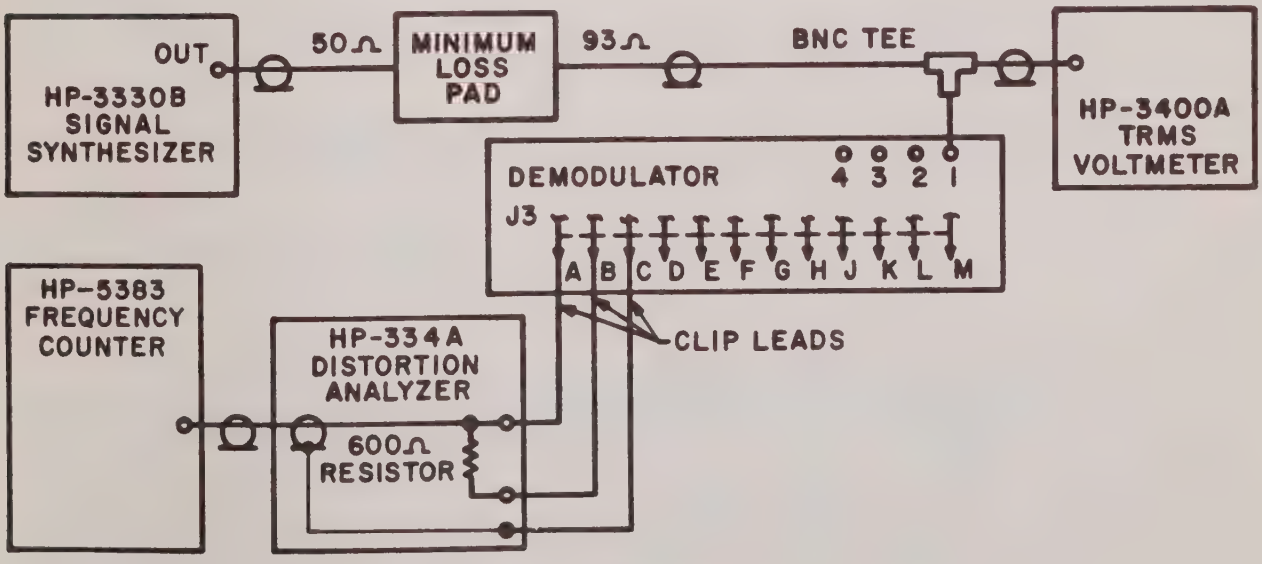


Figure 5-7. Adjustment Setup, Tuning Voltages, Resolution, Range, and Accuracy

3. Set Demodulator controls as follows:

   a. POWER - Off
   b. Rear Panel Routing Switches - BRDG position
   c. Phone LEVEL - Max. CCW
   d. DEMODULATOR SELECT - 1

4. Set Demodulator POWER switch to ON position, demodulator unit to LOCAL, 000.00 kHz, ERECT, and in AGC mode.

5. Install demodulator unit fine loop assembly A1A1 on extender card.

6. While using digital voltmeter to monitor tuning voltage at E1 on fine loop assembly, adjust capacitor C16 for a voltage level of -4.5 Vdc ±0.2 Vdc.

7. Remove fine loop assembly from extender card; remove extender card from demodulator unit; and reinstall fine loop assembly.

8. Install demodulator unit coarse loop assembly A1A2 on extender card and using control unit ERECT/INVERT switch, change demodulator unit from Erect to Invert mode.

9. While using digital voltmeter to monitor tuning voltage at E1 on coarse loop assembly, adjust capacitor C12 for a voltage level of -4.5 Vdc ±0.2 Vdc.

10. Remove coarse loop assembly from extender card; remove extender card from demodulator unit; and reinstall coarse loop assembly.

11. Install demodulator unit, main loop assembly A1A3 on extender card.

12. While using digital voltmeter to monitor tuning voltage at E1 on main loop assembly, adjust capacitor C16 for a voltage level of -4.5 Vdc ±0.2 Vdc.

13. Remove main loop assembly from extender card; remove extender card from demodulator unit; and reinstall main loop assembly.

14. Set Demodulator POWER switch to off position; remove demodulator unit from extender/test adapter; reinstall demodulator unit protective cover; and reinstall demodulator unit in Demodulator.

15. Set Demodulator POWER switch to ON position and tune demodulator unit to 308.00 kHz.

16. Set signal synthesizer output frequency to 309.00 kHz and output level of 17.5 mV as indicated on TRMS voltmeter.

NOTE

The outputs from AUDIO OUTPUT connector J3 are grouped as follows:

1 - A, B, and C (gnd)
2 - D, E, and F (gnd)
3 - G, H, and J (gnd)
4 - K, L, and M (gnd)

17. Using frequency counter, measure the output frequency from AUDIO OUTPUT connector J3. The output frequency is 3000 Hz ±5 Hz.

18. Tune demodulator unit to 123.45 kHz.

19. Set signal synthesizer output frequency to 124.68 kHz and output level of 17.5 mV as indicated on TRMS voltmeter.

20. Using frequency counter, measure the output frequency from AUDIO OUTPUT connector J3. The output frequency is 2770 Hz ±5 Hz.

21. Using control unit ERECT/INVERT switch, change demodulator unit from Invert to Erect mode.

22. Tune demodulator unit to 000.00 kHz.

23. Set signal synthesizer output frequency to 1.000 kHz and output level of 17.5 mV as indicated on TRMS voltmeter.

24. Using frequency counter, measure the output frequency from AUDIO OUTPUT connector J3. The output frequency is 1000 Hz ±5 Hz.

25. Repeat steps 15 through 24, as required, for each remaining demodulator unit.

5.3.5 REPAIR TECHNIQUES

5.3.5.1 General

As a result of the Demodulator's high density component packaging, repair of a specific trouble or fault is limited to component, circuit board, or assembly replacement. The options available are to either make the repair locally or to return the faulty component, circuit board, or assembly to the factory for replacement or repair. Many of the Demodulator's modules and components can be removed for testing and replacement while in other cases, only complete circuit boards can be removed. Since component and assembly replacement are obvious upon inspection and the level of maintenance and repair capability vary, the following procedures are presented in general terms.

5.3.5.2 Printed Circuit Board and Assembly Removal, Installation

Removal/replacement of printed circuit boards from their respective motherboards in the control unit and demodulator units is obvious and removal/replacement of the Baseband Signal Distribution Amplifier (A1A1) from the rear panel of the control rack frame is simply a matter of removing the attaching hardware and disconnecting the associated electrical interfaces. However, the Power Supply Assembly (A1A2), located in the control rack frame beside the control unit is unique. To remove/replace the Power Supply Assembly, remove the control unit and loosen the two quarter-turn fasteners on the rear end. Then, swing the rear-hinged board outward to a convenient angle and remove the board.

5.3.5.3 Component Removal

When removing components from a printed circuit board for inspection, testing, or replacement, be careful not to damage the tracks (conductors). Use a soldering iron with a power rating of 40 watts, or less, in conjunction with either a solder sipper or wicking procedure. If using a wicking procedure, be sure to use non-corrosive soldering flux. If possible, use a heat sink or long-nose pliers between the component being removed and hot soldering iron.

5.3.5.4 Component Installation

When installing components on a printed circuit board after inspection, testing, or as replacement parts, be sure lead connection holes are clear and free of excess solder prior to installing the components. When positioning components back in their original positions or installing new replacement components, do not force component leads into connection holes. Be sure that component leads do not catch on any track edges and cause tracks to be lifted from the board or cause any track damage. The soldering technique used should involve the same size soldering iron as in component removal, along with only enough heat and solder (60/40 rosin core) required to achieve good solder joints. If possible, use a heat sink or long-nose pliers between the component being installed and the hot soldering iron.

5.3.5.5 Printed Circuit Board Repair and Cleaning

Printed circuit boards may be repaired and cleaned locally using the procedures in this paragraph, or they may be replaced with another board while the defective board is being repaired at another facility. Repair damaged tracks using the following procedures or accepted local procedure.

1. Remove protective covering from undamaged track on both sides of damaged area. Allow overlap.

2. Bridge the damaged area using a length of tinned copper wire. Ensure that added bridge does not contact any other track or component lead.

Remove corrosion from printed circuit boards using a stiff bristled brush and 1, 1, 1-trichloroethane (methyl chloroform), or equivalent (see WARNING PAGE at front of this document for personnel hazards involving use of 1, 1, 1-trichloroethane).

SECTION VI

REPLACEMENT PARTS LIST

6.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation A1	R1 Class and No. of Item
Identify from right to left as:	First (1) resistor (R) of first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

6.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

6.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address
01037	Pyroferric-New York Inc. 621 E. 216th Street Bronx, NY 10467
01121	Allen-Bradley Company 1201 South 2nd Street Milwaukee, WI 53204
01295	Texas Instruments, Inc. Semiconductor-Components Div. 13500 North Central Expressway Dallas, TX 75231
02660	Bunker-Ramo Corporation Amphenol Connector Div. 2801 South 25th Avenue Broadview, IL 60153
02735	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876
03508	General Electric Company Semiconductor Products Dept. Electronics Park Syracuse, NY 13201
04713	Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85008
06540	Amatom Electronic Hardware Division of Mite Corp. 446 Blake Street New Haven, CT 06515

Mfr. Code	Name and Address
06776	Robertson-Nugent Inc. 800 E. 8th Street P.O. Box 270 Albany, IN 47150
07263	Fairchild Camera and Instrument Corp. Semiconductor Division 464 Ellis Street Mt. View, CA 94040
09021	Airco Electronics Foster Brook Road P.O. Box 334 Bradford, PA 16701
09353	C&K Components, Inc. 103 Morse Street Watertown, MA 02172
12498	Teledyne Crystalonics 147 Sherman Street Cambridge, MA 02140
13103	Thermalloy Company 2021 W. Valley View Lane Dallas, TX 75234
14632	Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, Maryland 20878
15542	Mini-Circuits Laboratory Division of Scientific Components Corporation 2913 Quentin Road Brooklyn, NY 11229
16179	Omni-Spectra Incorporated 24600 Hallwood Court Farmington, MI 48024
17856	Siliconix, Incorporated 2201 Lauralwood Road Santa Clara, CA 95050
19209	General Electric Company Battery Business Dept. P.O. Box 114 Gainsville, FL 32602
19505	Applied Engineering Products, Company Div. of Samarius Inc. 300 Seymour Avenue Derby, CT 06418
21604	The Buckeye Stamping Co. 555 Marion Road Columbus, OH 43207
22526	Berg Electronics, Inc. York Expressway New Cumberland, PA 17070
24355	Analog Devices, Inc. P.O. Box 280 Norwood, MA 02062
25088	Siemens America, Inc. 186 Wood Avenue S. Iselin, NJ 08830
27014	National Semiconductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27193	Cutler-Hammer, Inc. Specialty Products Div. 402 North 27th Street Milwaukee, WI 53216
28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304
28875	IMC Magnetics Corporation New Hampshire Division Route 16 Rochester, NH 03867

Mfr. Code	Name and Address
32293	Intersil, Incorporated 10900 North Tantau Ave. Cupertino, CA 95014
33095	Spectrum Control Inc. 152 E. Main Street Fairview, PA 16415
34371	Harris Semiconductor Div. Harris-Intertype Corp. P.O. Box 883 Melbourne, FL 32901
34649	Intel Corporation 3065 Bowers Ave. Santa Clara, CA 95051
49956	Raytheon Company 141 Spring Street Lexington, MA 02173
50579	Litronix Incorporated 19000 Homestead Road Cupertino, CA 95014
52072	Circuit Assembly Corp. 3169 Redhill Avenue Costa Mesa, CA 92626
52648	Plessey Semiconductors 1641 Kaiser Irvine, CA 92714
55322	Samtec Incorporated 810 Progress Blvd. P.O. Box 637 New Albany, IN 47150
56289	Sprague Electric Co. Marshall Street North Adams, MA 01247
71279	Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 02138
71400	Bussman Manufacturing Division of McGraw-Edison Company 2536 W. University Street St. Louis, MO 63107
71450	CTS Corporation 1142 W. Beardsley Ave. Elkhart, IN 46514
71468	ITT Cannon Electric 666 East Dyer Road Santa Ana, CA 92702
71785	TRW Electronic Components Cinch Connector Operations 1501 Morse Avenue Elk Grove Village, IL
72136	Electro Motive Manufacturing Company, Incorporated South Park & John Streets Willimantic, CT 06226
72619	Dialight Corporation Subsidiary of Digitronics Corporation 60 Stewart Avenue Brooklyn, NY 11237
72982	Erie Technological Products, Incorporated 644 West 12th Street Erie, PA 16512
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Blvd. Fullerton, CA 92634
74868	Bunker Ramo Corporation The Amphenol RF Division 33 East Franklin Street Danbury, CT 06810

Mfr. Code	Name and Address
75042	TRW Electronic Components IRC Fixed Resistors Philadelphia Division 401 North Broad Street Philadelphia, PA
75378	CTS Knights Inc. 400 Reimann Avenue Sandwich, IL 60548
75915	Littlefuse, Incorporated 800 E. Northwest Highway Des Plaines, IL 60016
77820	Bendix Corporation Electrical Components Div. Sherman Avenue Sidney, NY 13838
80058	Joint Electronics Type Designation System
80103	Lambda Electronics Corp. Division of Veeco Instruments Incorporated 515 Broad Hollow Road Melville, NY 11746
80131	Electronics Industries Assoc. 2001 Eye Street, N.W. Washington, DC 20006
81312	Winchester Electronics Div. Litton Industries, Inc. Main Street & Hillside Ave. Oakville, CT 06779
81349	Military Specifications
82389	Switchcraft, Inc. 5555 North Elston Ave. Chicago, IL 60630
82877	Rotron, Incorporated 7-9 Hasbrouck Lane Woodstock, NY 12498
83330	Herman H. Smith, Inc. 812 Snediker Avenue Brooklyn, NY 11207
91293	Johanson Manufacturing Co. P.O. Box 329 Boonton, NJ 07005
91506	Augat, Incorporated 33 Perry Avenue Attleboro, MA 02703
91833	Keystone Electronics Corp. 49 Bleecker Street New York, NY 10012
92825	Whitso Incorporated 9330 Byron Street Schiller Park, IL 60176
93332	Sylvania Electric Products, Incorporated Semiconductor Products Div. 100 Sylvan Road Woburn, MA 01801
95121	Quality Components, Inc. P.O. Box 113 St. Mary's, PA 15857
96906	Military Standards
98291	Sealectro Corporation 225 Hoyt Mamaroneck, NY 10544

Mfr. Code	Name and Address
98978	International Electronic Research Corporation 135 West Magnolia Blvd. Burbank, CA 91502
99800	American Precision Industries Industries, Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052

6.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from the Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in paragraph 6.3 and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semiconductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes and integrated circuits installed in the equipment may not agree with those specified in the parts lists and schematic diagrams of this manual. However, the semiconductors designated in the manual may be substituted in every case with satisfactory results.

6.5 TYPE WJ-9525 DEMODULATOR, MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
A1	Control Rack Frame	1	WJ-9525/CRF	14632	
A2	Control Unit	1	WJ-9525/CU	14632	
A3	Demodulator Unit	4	WJ-9525/DU	14632	
A4 Thru A6	Same as A3				

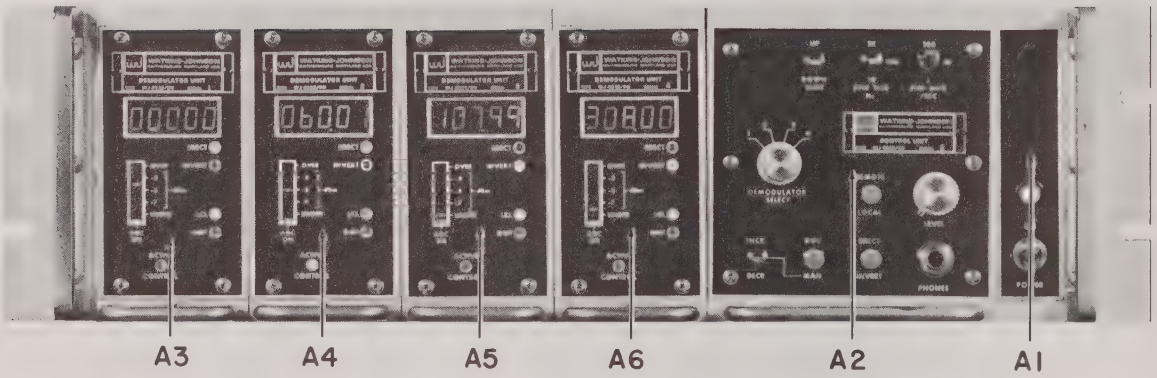


Figure 6-1. WJ-9525 Demodulator, Front View, Location of Components

6.5.1 TYPE WJ-9525/CRF CONTROL RACK FRAME REF DESIG PREFIX A1

REF DESIG	DESCRIPTION		QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Assembly Revision C					
A1	Baseband Amplifier		1	796074	14632	
A2	Power Supply		1	766001	14632	
A3	Reference Generator		1	796060	14632	
B1	Fan, Blower: 115 Vac, 0.08 Amp, 50/60 Hz, 75 CFM		1	WR2H1	82877	
C1	Capacitor, Electrolytic, Tantalum: 4.7 µF, 10%, 35 V		8	CS13BF475K	81349	56289
C2	Same as C1					
C3	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V		1	196D475X0035JE3	56289	
C4 Thru C9	Same as C1					
DS1	Lamp Assembly, Neon		1	249-7841-1431-574	72619	
E4	Terminal, Standoff		8	7A1A1	92825	
E5 Thru E9	Same as E4					
E12	Same as E4					
E13	Same as E4					
E30	Same as E4					
E31	Same as E4					
F1	Fuse, Cartridge, 3AG Slow-blow: 1.5 Amp		1	MDX1.5	71400	
F2	Fuse, Cartridge, 3AG Slow-blow: 3/4 Amp		1	MDL3/4	71400	
FL1	Filter, Power Line		1	23977-1	14632	
J1	Connector, Jack, BNC Series	Part of W1	1	30517-10	77820	
J2	Connector, Receptacle, Multipin	Part of W18	1	57-20240-2	02660	
J3	Connector, Receptacle, Multipin	Part of W18	1	MS3112E14-19S	96906	77820
J4	Connector, Printed Circuit Card		4	252-22-30-160	71785	
J5	Same as J4					
J6	Same as J4					
J7	Same as J4					
J8	Connector, Receptacle Multipin		1	DD50SE	71468	
J9	Connector, Receptacle Multipin	Part of W18	1	DBM25S	71468	
MP1	Handle, Front Panel		2	32306-1	14632	
MP2	Handle, Rear Panel		2	415-1270-01-18	71279	
MP3	Connector Hood		1	SM3H	81312	
MP4	Cover, Top		1	480160	14632	
MP5	Cover, Bottom		1	480163	14632	
MP6	Filter Screen, Blower		1	69-93	28875	
MP7	Cover, Voltage Regulator		1	4632	91833	
P1	Connector, Multipin		1	SM3SN	81312	
P2	Connector, Plug, SMC Series	Part of W2	9	UG1466/U	80058	19505
P3	Same as P2	Part of W3				

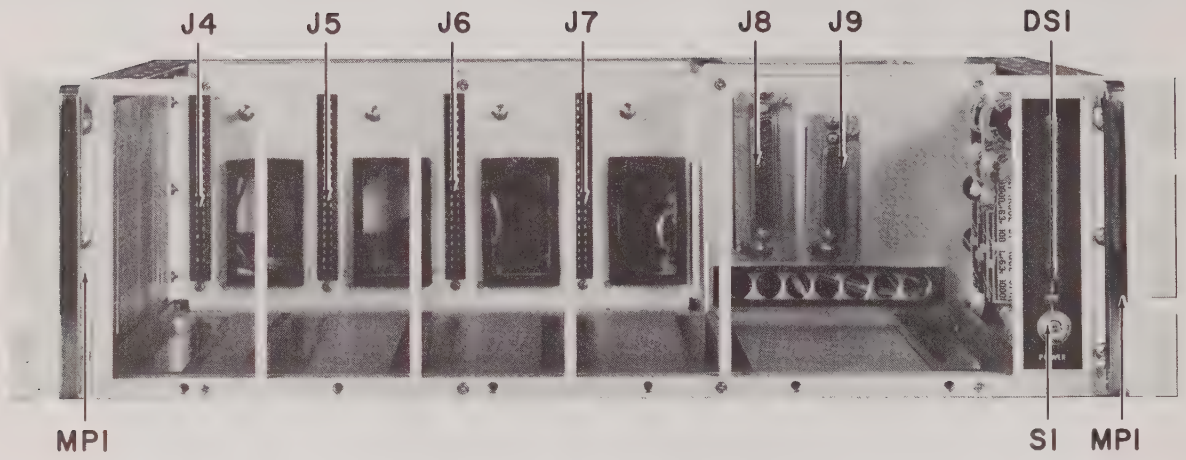


Figure 6-2. WJ-9525/CRF Control Rack Frame (A1), Front View, Location of Components

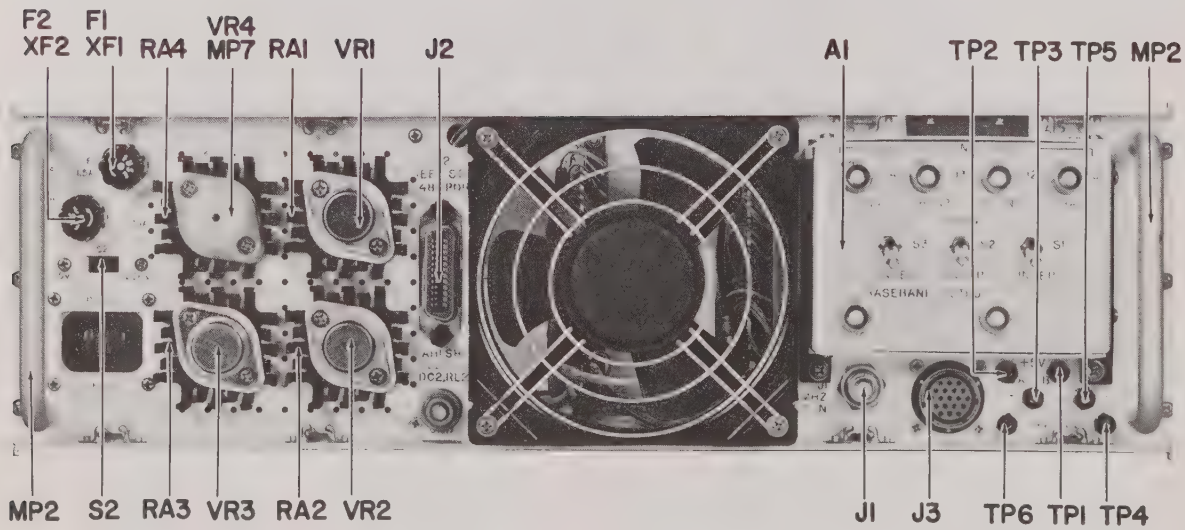


Figure 6-3. WJ-9525/CRF Control Rack Frame (A1), Rear View, Location of Components

REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
P4	Same as P2 Part of W4				
P5	Same as P2 Part of W5				
P6	Same as P2 Part of W1				
P7	Same as P2 Part of W7				
P8	Same as P2 Part of W8				
P9	Same as P2 Part of W9				
P10	Same as P2 Part of W10				
P13	Connector, Plug, Faston	2	42236-1	00779	
P14	Same as P13				
P15	Connector, Plug, Faston	14	2-350804-2	00779	
P16 Thru P28	Same as P15				
RA1	Heat Sink	4	UP2-T03-CB	98978	
RA2	Same as RA1				
RA3	Same as RA1				
RA4	Same as RA1				
S1	Switch, Toggle: DPST	1	8370K8	27193	
S2	Switch, Slide: DPDT	1	11A1211	82389	
T1	Power Transformer	1	380090	14632	
TP1	Test Jack	6	1501-103	83330	
TP2 Thru TP6	Same as TP1				
VR1	Voltage Regulator	2	LAS1905	80103	
VR2	Same as VR1				
VR3	Voltage Regulator	1	LAS15A15	80103	
VR4	Voltage Regulator	1	LAS18A15	80103	
W1	Cable Assembly	1	380125-1	14632	
W2	Cable Assembly	1	380124-1	14632	
W3	Cable Assembly	1	380124-2	14632	
W4	Cable Assembly	1	380124-3	14632	
W5	Cable Assembly	1	380124-4	14632	
W6	Not Used				
W7	Cable Assembly	1	380124-5	14632	
W8	Cable Assembly	1	380124-6	14632	
W9	Cable Assembly	1	380124-7	14632	
W10	Cable Assembly	1	380124-8	14632	
W11 Thru W16	Not Used				
W17	Power Line Cable	1	17250	16428	
W18	Cable Assembly	1	380126-1	14632	

REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
XA2	Connector, Printed Circuit Card	1	251-15-30-160	71785	
XF1	Fuseholder	2	342004	75915	
XF2	Same as XF1				
XVR1	Socket, Voltage Regulator	4	8080-1G1	91506	
XVR2	Same as XVR1				
XVR3	Same as XVR1				
XVR4	Same as XVR1				
---	Accessory Items ---				
AI1	Connector, Plug, Multipin	1	MS3116B14-19P	96906	77820
---	Cable Assembly	1	380128	14632	
---	Extender Plate Assembly	1	380129	14632	

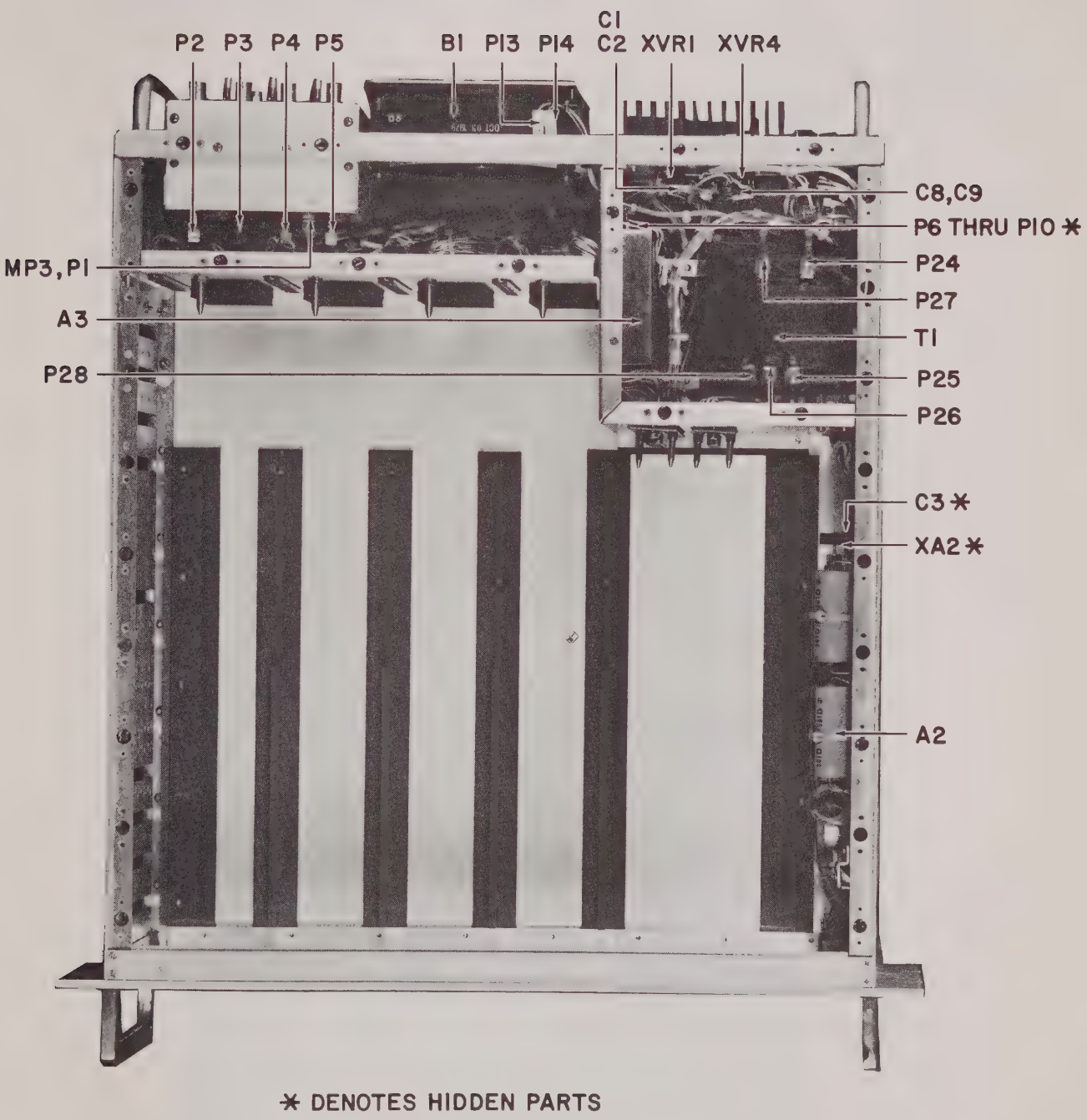


Figure 6-4. WJ-9525/CRF Control Rack Frame (A1), Top View, Location of Components

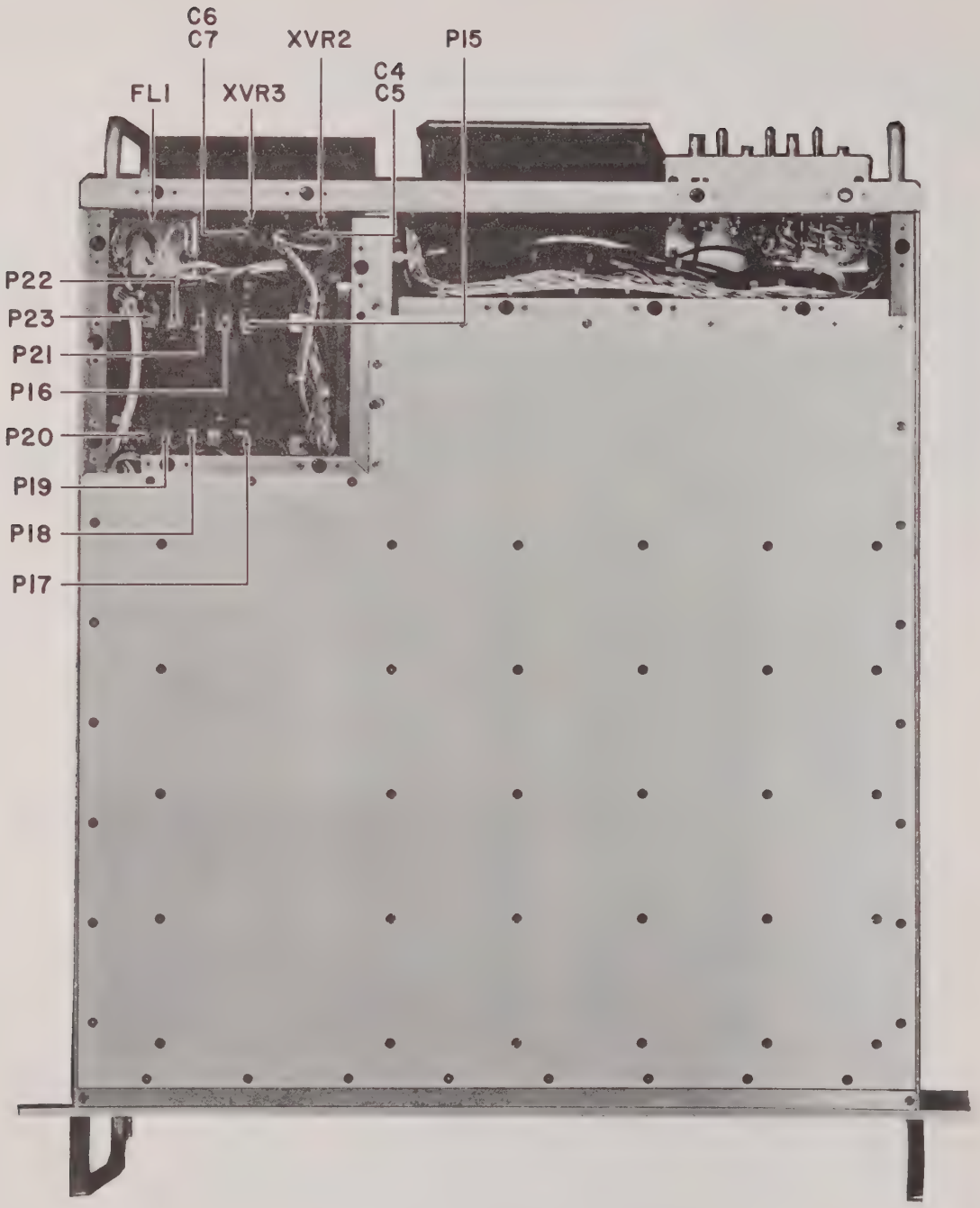


Figure 6-5. WJ-9525/CRF Control Rack Frame (A1), Bottom View, Location of Components

6.5.1.1 Type 796074 Baseband Signal Distribution Amplifier REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
A1	Baseband Distribution Amplifier	2	796065	14632	
A2	Same as A1				
J1	Connector, Receptacle: BNC Series	6	UG1094/U	80058	74868
J2 Thru J6	Same as J1				
J7	Connector, Receptacle	4	UG1619	80058	74868
J8	Same as J7				
J9	Same as J7				
J10	Same as J7				
J11	Connector, Multipin	1	SM3P	81312	
MP1	Cover Assembly	1	480167	14632	
S1	Switch, Toggle: SPDT	3	7101	09353	
S2	Same as S1				
S3	Same as S1				

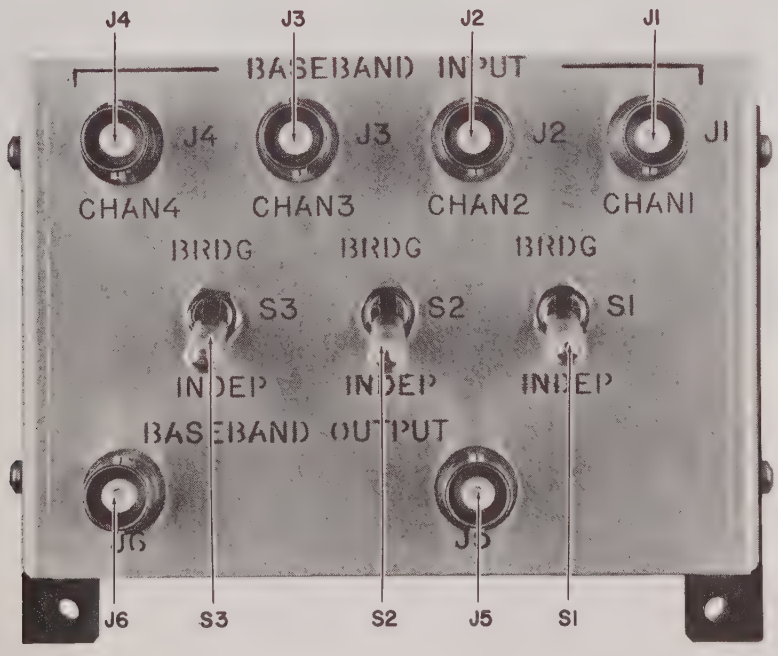


Figure 6-6. Type 796074 Baseband Signal Distribution Amplifier (A1A1), Front View, Location of Components

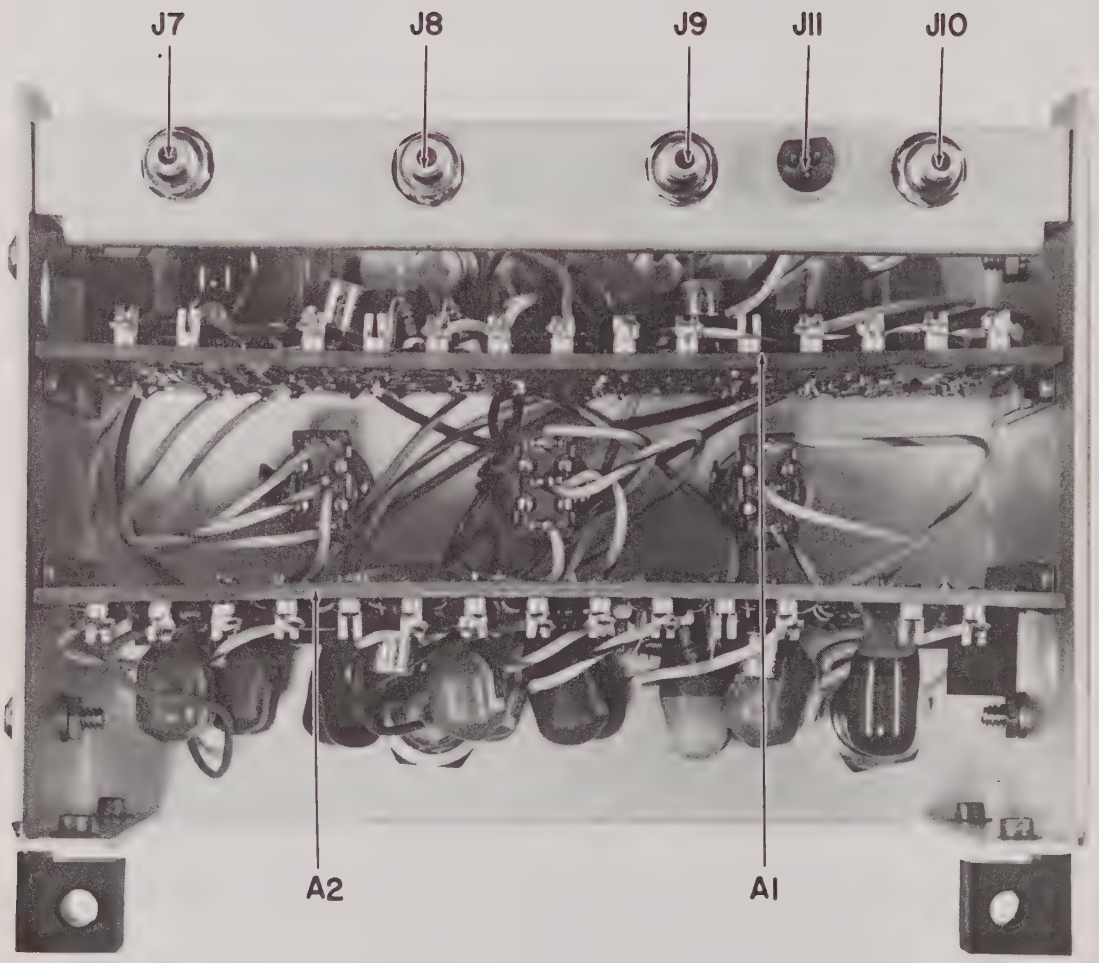


Figure 6-7. Type 796074 Baseband Signal Distribution Amplifier (A1A1), Rear View, Location of Components

6.5.1.1.1 Part 796065 Baseband Distribution Amplifier REF DESIG PREFIX A1A1A1, A1A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	2	196D476X0020PE4	56289	
C2	Same as C1				
C3	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	10	196D107X0020TE4	56289	
C4	Same as C3				
C5	Same as C3				
C6	Capacitor, Ceramic, Disc: 10 pF, ±0.25 pF, 50 V	2	8101-050C0G0-100C	72982	
C7	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 35 V	2	196D476X0035TE4	56289	
C8	Same as C3				
C9	Same as C3				
C10	Same as C3				
C11	Same as C6				
C12	Same as C3				
C13	Same as C7				
C14	Same as C3				
C15	Same as C3				
C16	Same as C3				
CR1	Diode	6	1N4444	80131	03508
CR2 Thru CR6	Same as CR1				
MP1	Transipad	2	7717-46DAP	13103	
Q1	Transistor	2	2N2222A	80131	04713
Q2	Same as Q1				
R1	Resistor, Fixed, Film: 93.1 Ω, 1%, 1/4 W	2	CC93R1F	01121	
R2	Resistor, Fixed, Film: 6.81 kΩ, 1%, 1/4 W	4	CC6811F	01121	
R3	Resistor, Fixed, Film: 120 Ω, 5%, 1/8 W	4	CF1/8-120Ω/J	09021	
R4	Resistor, Fixed, Film: 51.1 Ω, 1%, 1/4 W	4	CC51R1F	01121	
R5	Resistor, Fixed, Film: 20 Ω, 5%, 1/8 W	4	CF1/8-20Ω/J	09021	
R6	Same as R4				
R7	Same as R5				
R8	Same as R2				
R9	Same as R3				
R10	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	10	CF1/8-47Ω/J	09021	
R11	Same as R10				
R12	Resistor, Fixed, Film: 27 Ω, 5%, 1/8 W	10	CF1/8-27Ω/J	09021	
R13	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	2	CF1/8-2.2kΩ/J	09021	
R14	Same as R12				
R15	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	2	CF1/8-3.3kΩ/J	09021	
R16	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	4	CF1/8-1kΩ/J	09021	
R17	Same as R16				
R18	Same as R10				

REF DESIG PREFIX A1A1A1, A1A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R19	Same as R10				
R20	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	2	CF1/8-470Ω/J	09021	
R21	Same as R10				
R22	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	2	CF1/8-22kΩ/J	09021	
R23	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	2	CF1/8-10kΩ/J	09021	
R24	Same as R12				
R25	Same as R12				
R26	Same as R2				
R27	Same as R3				
R28	Same as R4				
R29	Same as R5				
R30	Same as R4				
R31	Same as R5				
R32	Same as R2				
R33	Same as R3				
R34	Same as R10				
R35	Same as R10				
R36	Same as R12				
R37	Same as R13				
R38	Same as R12				
R39	Same as R15				
R40	Same as R16				
R41	Same as R16				
R42	Same as R10				
R43	Same as R10				
R44	Same as R20				
R45	Same as R10				
R46	Same as R22				
R47	Same as R23				
R48	Same as R12				
R49	Same as R12				
R50	Same as R12				
R51	Resistor, Fixed, Film: 12.1 kΩ, 1%, 1/4 W	2	CC1212F	01121	
R52	Resistor, Fixed, Film: 392 Ω, 1%, 1/4 W	2	CC3920F	01121	
R53	Resistor, Fixed, Film: 30.1 Ω, 1%, 1/4 W	2	CC30R1F	01121	
R54	Resistor, Fixed, Film: 200 Ω, 1%, 1/4 W	2	CC2000F	01121	
R55	Resistor, Fixed, Film: 100 Ω, 1%, 1/4 W	4	CC1000F	01121	
R56	Same as R55				
R57	Same as R54				
R58	Resistor, Variable, Film: 2 kΩ, 10%, 1/2 W	1	62PAR2K	73138	
R59	Resistor, Fixed, Film: 825 Ω, 1%, 1/4 W	1	CC8250F	01121	

REF DESIG PREFIX A1A1A1, A1A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R60	Same as R55				
R61	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	1	CF1/8-10Ω/J	09021	
R62	Same as R55				
R63	Same as R51				
R64	Same as R52				
R65	Same as R53				
R66	Same as R12				
R67	Same as R1				
U1	Transistor	5	MHQ6002	04713	
U2	Same as U1				
U3	Same as U1				
U4	Same as U1				
U5	Same as U1				

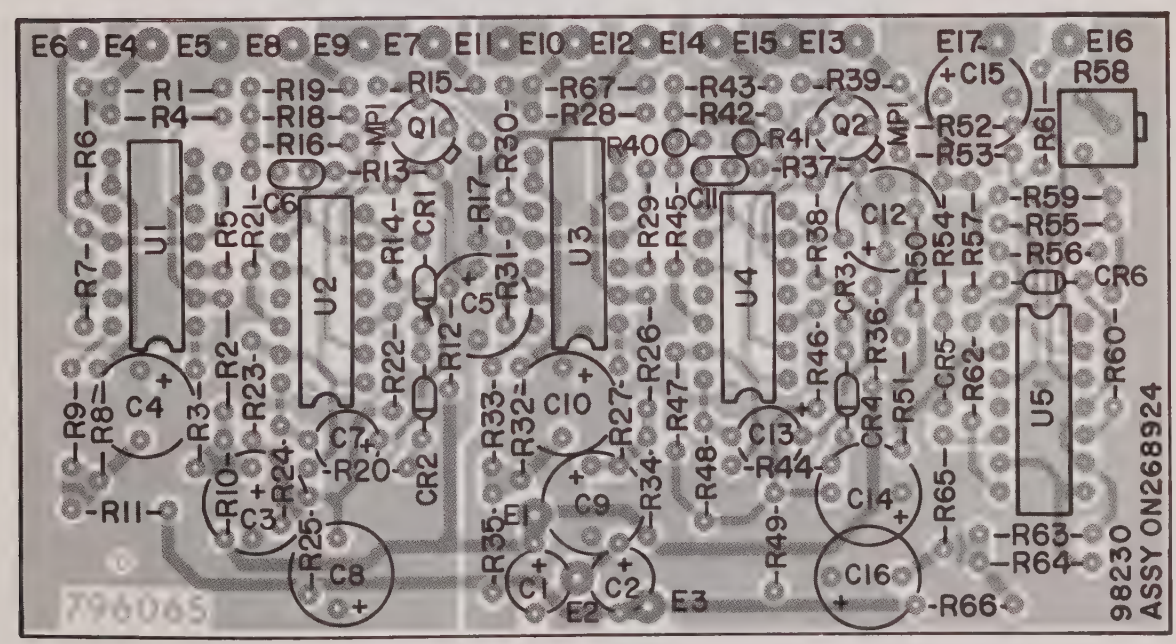


Figure 6-8. Type 796065 Baseband Distribution Amplifier (A1A1A1, A1A1A2), Location of Components

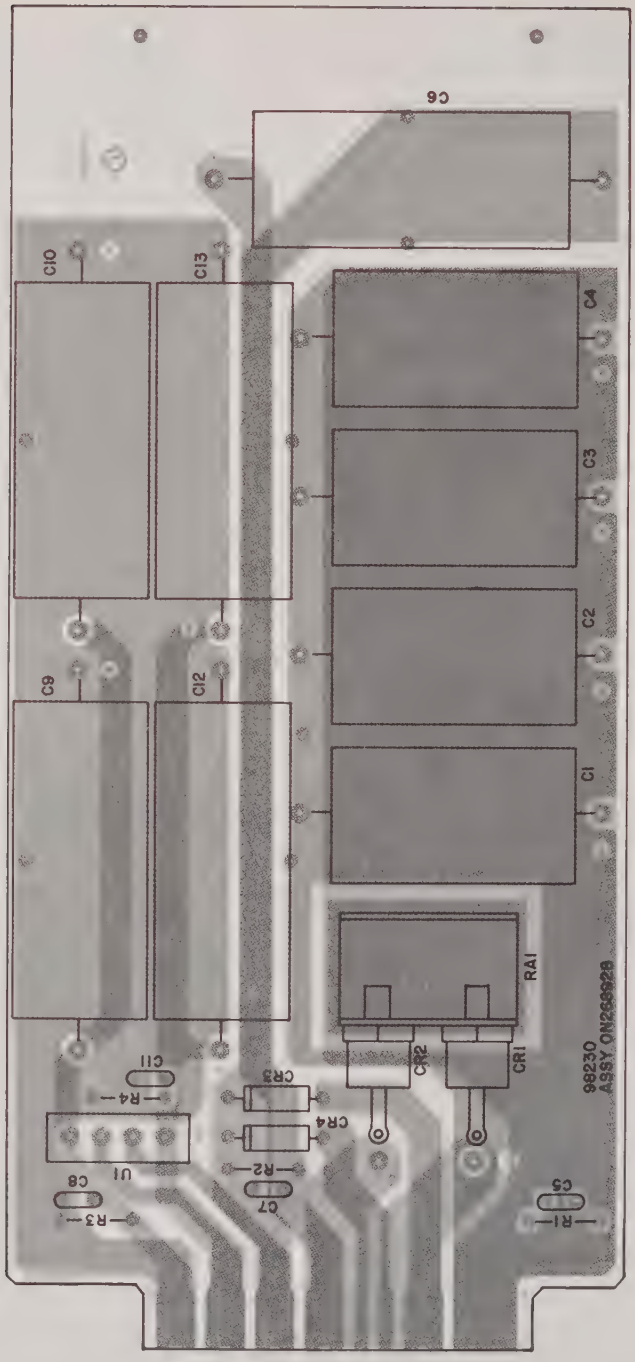


Figure 6-9. Type 766001 Power Supply (A1A2)
Location of Components

6.5.1.2 Type 766001 Power Supply REF DESIG PREFIX A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Electrolytic, Aluminum: 4700 µF, +50-10%, 16 V	4	501D478F016TV	56289	
C2	Same as C1				
C3	Same as C1				
C4	Same as C1				
C5	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	4	8131M100-651-104M	72982	
C6	Capacitor, Electrolytic, Aluminum: 10,000 µF, +50-10%, 6.3V	1	501D109F6R3TW	56289	
C7	Same as C5				
C8	Same as C5				
C9	Capacitor, Electrolytic, Aluminum: 3,300 µF, +50-10%,	4	501D338F035TW	56289	
C10	Same as C9				
C11	Same as C5				
C12	Same as C9				
C13	Same as C9				
CR1	Diode	2	1N5828	80131	04713
CR2	Same as CR1				
CR3	Diode	2	1N5821	80131	04713
CR4	Same as CR3				
R1	Resistor, Fixed, Composition: 1 kΩ, 5%, 1/4 W	2	RCR07G102JS	81349	01121
R2	Same as R1				
R3	Resistor, Fixed, Composition: 4.7 kΩ, 5%, 1/4 W	2	RCR07G472JS	81349	01121
R4	Same as R3				
RA1	Radiator	1	380116	14632	
U1	Rectifier	1	MDA970-2	04713	

6.5.1.3 Type 796060 Reference Generator Assembly REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
A1	Reference Generator	1	380084	14632	
C1	Capacitor, Ceramic, Feedthru: 0.05 µF, GMV, 300 V	3	54-785-002-503P	33095	
C2	Same as C1				
C3	Same as C1				
J1	Connector, Receptacle: SMC Series	5	UG1464/U	80058	19505
J2	Same as J1				
J3	Same as J1				
J4	Same as J1				
J5	Same as J1				

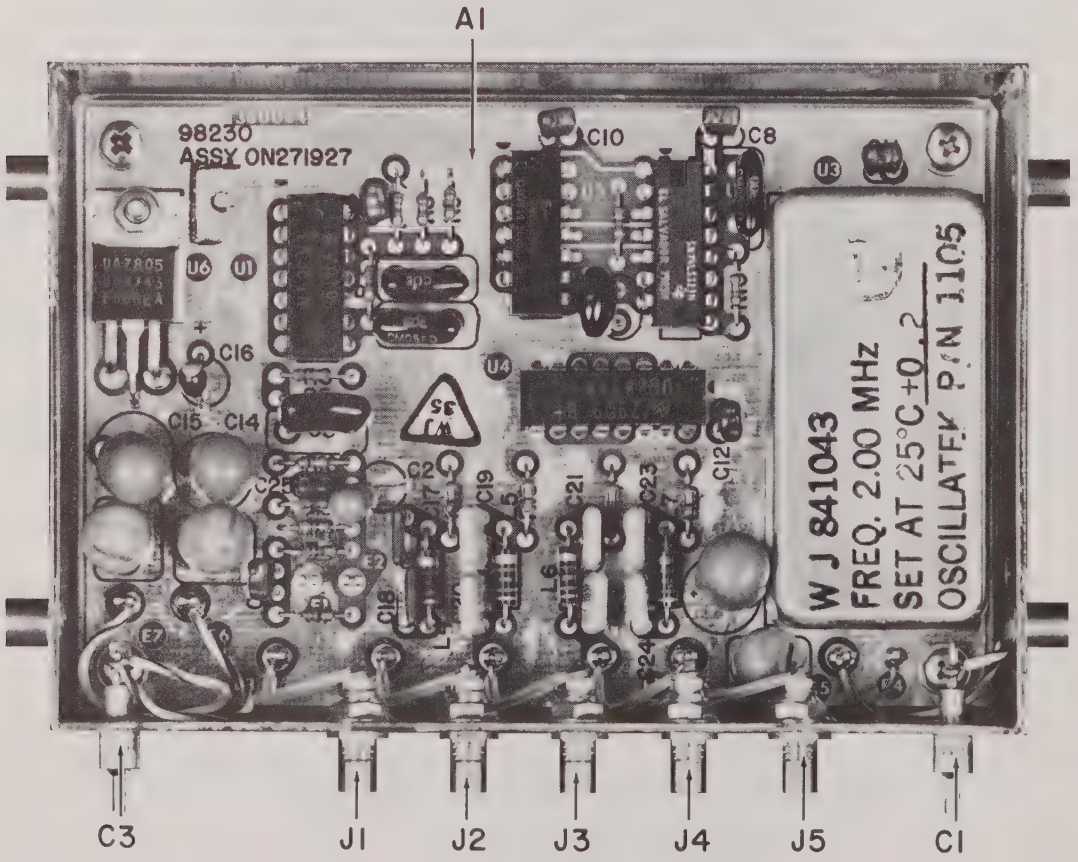


Figure 6-10. Type 796060 Reference Generator Assembly (A1A3), Top View, Location of Components

6.5.1.3.1 Part 380084 Reference Generator REF DESIG PREFIX A1A3A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	6	8121-050-651-104M	72982	
C2	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	1	196D186X9020KE3	56289	
C3	Capacitor, Mica, Dipped: 750 pF, 5%, 300 V	1	DM15-751J	72136	
C4	Same as C1				
C5	Capacitor, Mica, Dipped: 150 pF, 2%, 500 V	2	CM05FD151G03	81349	72136
C6	Same as C5				
C7	Capacitor, Mica, Dipped: 82 pF, 2%, 500 V	1	CM05ED820G03	81349	72136
C8	Same as C1				
C9	Capacitor, Mica, Dipped: 330 pF, 2%, 100 V	1	CM04FA331G03	81349	72136
C10	Same as C1				
C11	Same as C1				
C12	Same as C1				
C13	Capacitor, Electrolytic, Tantalum: 220 µF, 20%, 10 V	1	196D227X0010TE4	56289	
C14	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	2	196D476X0020PE4	56289	
C15	Same as C14				
C16	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	1	196D105X0035HE3	56289	
C17	Capacitor, Ceramic, Disc: 2200 pF, 5%, 50 V	8	8131-050C0G0-222J	72982	
C18 Thru C24	Same as C17				
C25	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	1	8121-050-651-103M	72982	
L1	Coil, Fixed: 680 µH	1	553-3635-35	71279	
L2	Coil, Fixed: 47 mH	1	553-3635-57	71279	
L3	Coil, Fixed: 22 mH	1	553-3635-53	71279	
L4	Coil, Fixed: 6.8 µH	4	1025-40	99800	
L5	Same as L4				
L6	Same as L4				
L7	Same as L4				
R1	Resistor, Fixed, Film: 51 Ω, 5%, 1/8 W	1	CF1/8-51Ω/J	09021	
R2	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	1	CF1/8-1kΩ/J	09021	
R3	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15kΩ/J	09021	
R4	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	5	CF1/8-47Ω/J	09021	
R5	Resistor, Fixed, Film: 200 Ω, 5%, 1/8 W	1	CF1/8-200Ω/J	09021	
R6	Resistor, Fixed, Film: 7.5 kΩ, 5%, 1/8 W	1	CF1/8-7.5kΩ/J	09021	
R7	Resistor, Fixed, Film: 6.2 kΩ, 5%, 1/8 W	2	CF1/8-6.2kΩ/J	09021	
R8	Resistor, Fixed, Film: 560 Ω, 5%, 1/8 W	2	CF1/8-560Ω/J	09021	
R9	Same as R8				
R10	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	1	CF1/8-4.7kΩ/J	09021	
R11	Resistor, Fixed, Film: 20 kΩ, 5%, 1/8 W	1	CE1/8-20kΩ/J	09021	
R12	Same as R4				
R13	Same as R4				

REF DESIG PREFIX A1A3A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R14	Same as R4				
R15	Same as R4				
R16	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100Ω/J	09021	
R17	Same as R7				
U1	Integrated Circuit	1	LM361N	27014	
U2	Integrated Circuit	1	SN74LS123N	01295	
U3	Integrated Circuit	1	841043	14632	
U4	Integrated Circuit	1	D58831N	27014	
U5	Integrated Circuit	1	SN74LS02N	01295	
U6	Integrated Circuit	1	7805UC	07263	

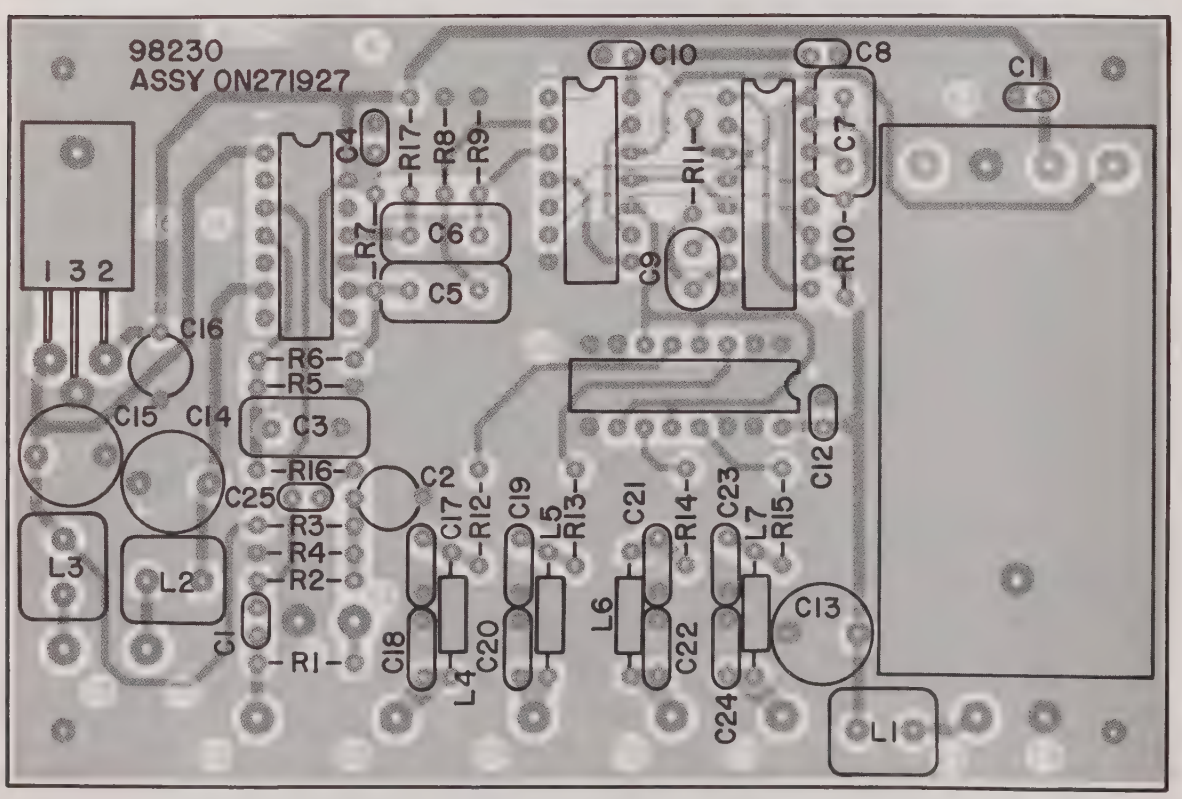


Figure 6-11. Part 380084 Reference Generator (A1A3A1), Location of Components

6.5.2 TYPE WJ-9525/CU CONTROL UNIT REF DESIG PREFIX A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
A1	Motherboard, Control Unit	1	796061	14632	
J1	Connector, Phone Jack	1	L11	82389	
J2	Connector, Receptacle, Multipin	1	DBM25P	71468	
J3	Connector, Receptacle, Multipin	1	DDM50P	71468	
MP1	Handle, Front Panel	1	10233-B-0632-4A	06540	
MP2	Knob, Round	1	PS50D1-LG	21604	
MP3	Screw, Captive Panel	2	6130SS0632	06540	
MP4	Switch Cap, Red	3	8018-3	09353	
MP5	Cover	1	480173	14632	
MP6	Knob, Round	1	PS70PL2-G	21604	
P1	Connector, Plug	1	65057-018	22526	
P2	Connector, Plug	1	65057-008	22526	
P3	Connector, Plug	1	65057-016	22526	
R1	Resistor, Variable, Composition: 2.5 kΩ, ±10%, 1/2 W	1	RV6NAYSD252A	81349	01121
S1	Switch, Toggle: SPDT	2	7105P3	09353	
S2	Same as S1				
S3	Switch, Pushbutton: SPDT	3	8121	09353	
S4	Switch, Toggle: SPDT	2	7103P3	09353	
S5	Same as S4				
S6	Same as S3				
S7	Same as S3				
S8	Switch, Rotary, Modified	1	1128-03	14632	
	Accesory Item				
--	Extender Board	1	796088	14632	

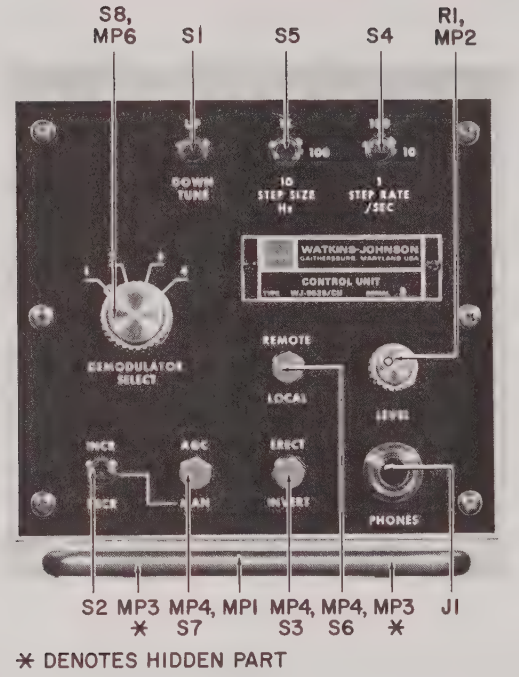


Figure 6-12. WJ-9525/CU Control Unit (A2), Front View, Location of Components

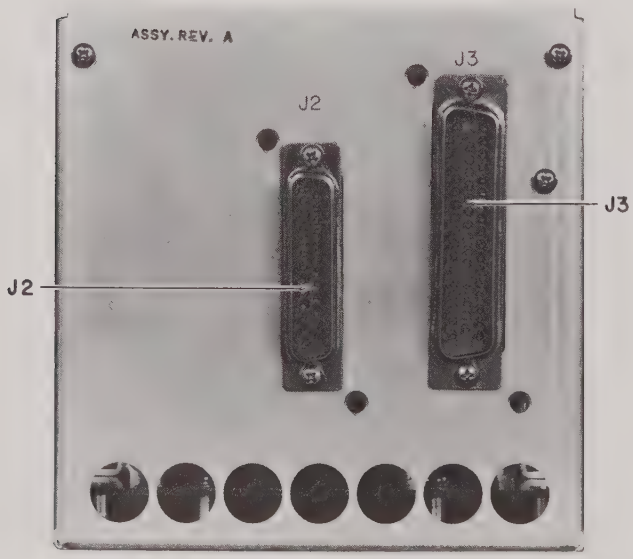


Figure 6-13. WJ-9525/CU Control Unit (A2), Rear View, Location of Components

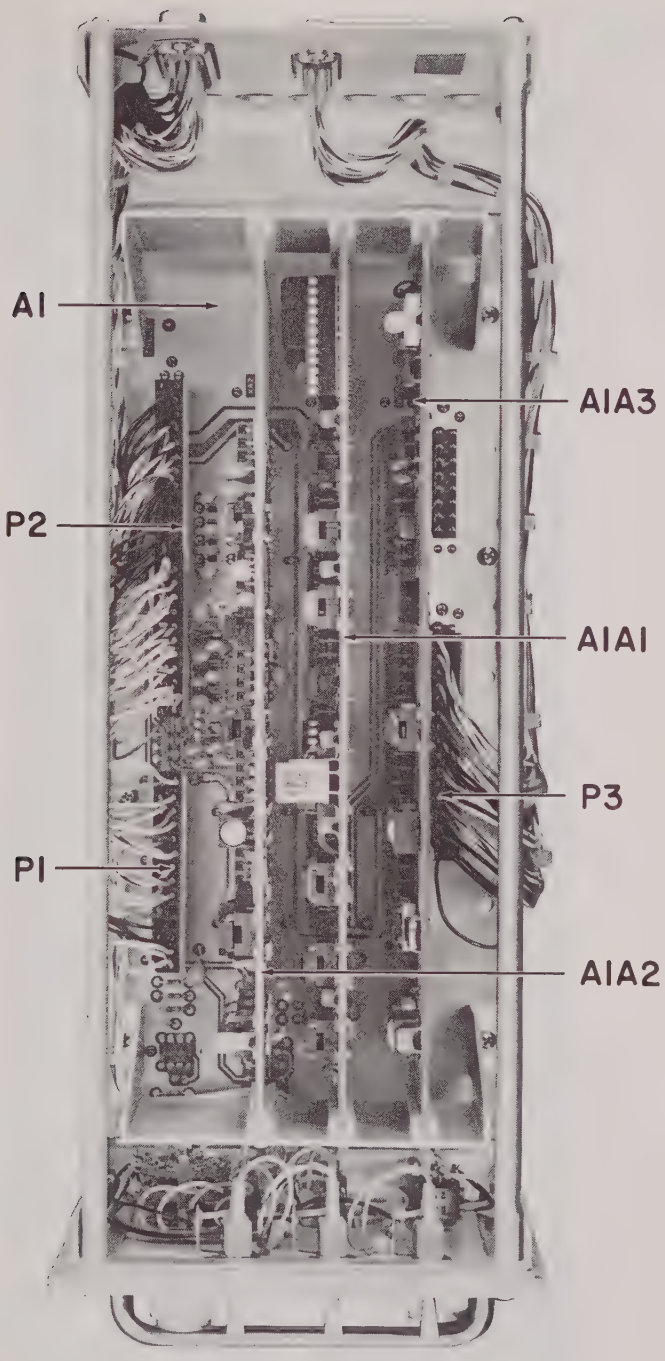


Figure 6-14. WJ-9525/CU Control Unit (A2), Top View, Location of Components

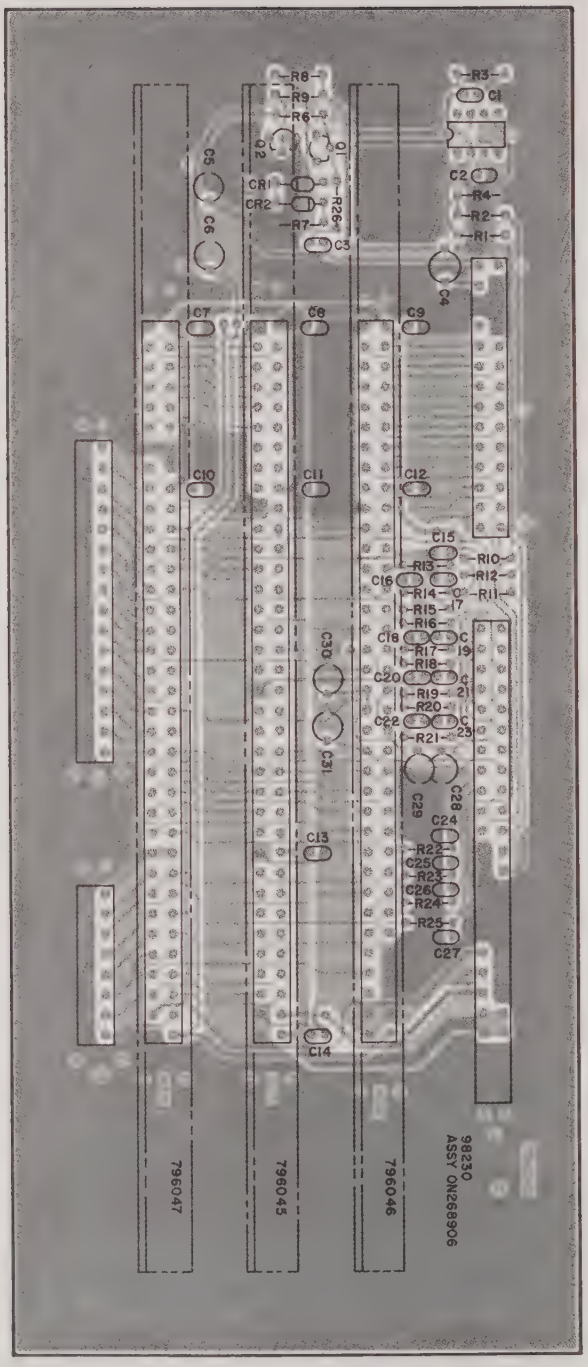


Figure 6-15. Type 796061 Motherboard, Control Unit (A2A1), Location of Components

6.5.2.1 Type 796061 Motherboard, Control Unit REF DESIG PREFIX A2A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Assembly Revision B				
A1	CPU Processor & Memory	1	796045	14632	
A2	Panel Interface/Demodulator Control	1	796046	14632	
A3	IEEE 488/RS-232 I/O Module	1	796047-1	14632	
C1	Capacitor, Ceramic, Disc: 470 pF, 10%, 50 V	2	8101-050X7R0-471K	72982	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	5	8121-050-651-104M	72982	
C4	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	7	196D186X9020KE3	56289	
C5	Same as C4				
C6	Same as C4				
C7	Same as C3				
C8	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	4	196D107X0020TE4	56289	
C9	Same as C8				
C10	Same as C8				
C11	Same as C3				
C12	Same as C3				
C13	Same as C3				
C14	Same as C8				
C15	Capacitor, Ceramic, Disc: 1000 pF, 20%, 50 V	13	8101-050-651-102M	72982	
C16 Thru C27	Same as C15				
C28 Thru C31	Same as C4				
CR1	Diode	2	1N1914/JAN	80131	93332
CR2	Same as CR1				
J1	Connector, Receptacle	1	1-87228-4	00779	
J2	Connector, Receptacle	1	2-87228-4	00779	
J3	Connector, Receptacle	1	1-87228-6	00779	
J4	Connector, Receptacle (Optional)	X	87228-8	00779	
Q1	Transistor	1	2N3904	80131	04713
Q2	Transistor	1	2N3906	80131	04713
R1	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	2	CF1/8-1kΩ/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 56 kΩ,5 %, 1/8 W	2	CF1/8-56kΩ/J	09021	
R4	Same as R3				
R5	Not Used				
R6	Resistor, Fixed, Film: 16 kΩ, 5%, 1/8 W	2	CF1/8-16kΩ/J	09021	
R7	Same as R6				

REF DESIG PREFIX A2A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R14 Thru R25	Same as R13				
R26	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470Ω/J	09021	
U1	Integrated Circuit	1	741TC	07263	
XA1P1A	Connector, Receptacle	6	1-87228-8	00779	
XA1P1B	Same as XA1P1A				
XA2P1A	Same as XA1P1A				
XA2P1B	Same as XA1P1A				
XA3P1A	Same as XA1P1A				
XA3P1B	Same as XA1P1A				

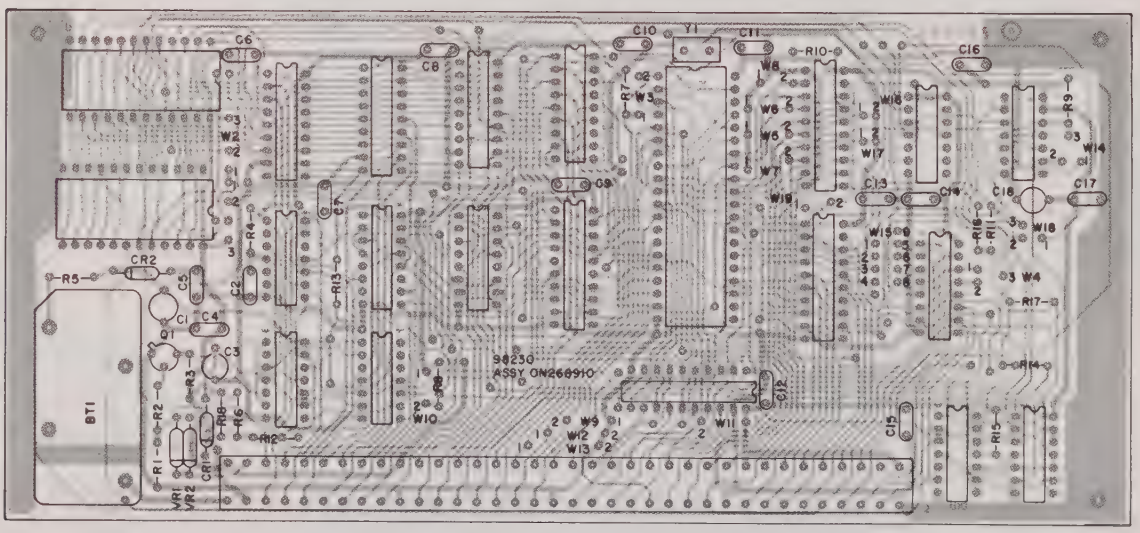


Figure 6-16. Type 796045 CPU Processor & Memory (A2A1A1), Location of Components

6.5.2.1.1 Type 796045 CPU Processor & Memory REF DESIG PREFIX A2A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
BT1	Battery, NI-CAD 3.6 V, 65 MA	1	DS3SD	19209	
C1	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	2	196D186X9020KE3	56289	
C2	Capacitor, Mica, Dipped: 500 pF, 5%, 500 V	1	DM15-501J	72136	
C3	Capacitor, Ceramic, Disc: 0.47 µF, ±20%, 50 V	1	34452-1	14632	
C4	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	14	8131M100-651-104M	72982	
C5 Thru C17	Same as C4				
C18	Same as C1				
CR1	Diode	1	1N462A	80131	93332
CR2	Diode	1	1N270	80131	93332
MP1	Transipad	1	7717-44DAP	13103	
P1	Connector, Receptacle	1	65002-057	22526	
Q1	Transistor	1	2N2222A	80131	04713
R1	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100kΩ/J	09021	
R2	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	3	CF1/8-1kΩ/J	09021	
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	5	CF1/8-10kΩ/J	09021	
R4	Resistor, Fixed, Film: 51 kΩ, 5%, 1/8 W	1	CF1/8-51kΩ/J	09021	
R5	Resistor, Fixed, Film: 200 Ω, 5%, 1/8 W	1	CF1/8-200Ω/J	09021	
R6	Same as R3				
R7	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470Ω/J	09021	
R8	Same as R3				
R9	Same as R3				
R10	Same as R3				
R11	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/8 W	1	CF1/8-8.2kΩ/J	09021	
R12	Same as R2				
R13	Same as R2				
R14	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	2	CF1/8-3.3kΩ/J	09021	
R15	Same as R14				
R16	Resistor, Fixed, Film: 5.6 kΩ, 5%, 1/8 W	1	CF1/8-5.6kΩ/J	09021	
R17*	Not Used				
R18	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100Ω/J	09021	
U1	Integrated Circuit	1	P8085A	34649	
U2	Integrated Circuit	1	841054	14632	
U3*	Not Used				
U4*	Not Used				
U5*	Not Used				
U6	Integrated Circuit	2	HM1-6561-9	34371	
U7	Same as U6				
*	R17, U3, U4, U5 are for future expansion, not used at this time.				

REF DESIG PREFIX A2A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U8	Integrated Circuit	1	SN74LS138N	01295	
U9	Integrated Circuit	1	SN74LS03N	01295	
U10	Integrated Circuit	1	SN74LS02N	01295	
U11	Integrated Circuit	1	CD40106BE	02735	
U12	Integrated Circuit	1	MC14081BCP	04713	
U13	Integrated Circuit	1	CD4013BE	02735	
U14	Integrated Circuit	1	SN74LS00N	01295	
U15	Integrated Circuit	1	SN74LS74N	01295	
U16	Integrated Circuit	2	P8216	34649	
U17	Integrated Circuit	2	SN74LS363N	01295	
U18	Same as U17				
U19	Integrated Circuit	2	SN74LS244N	01295	
U20	Same as U19				
U21	Same as U16				
VR1	Diode, Zener: 8.2 V	1	1N756A	80131	04713
VR2	Diode, Zener: 5.1 V	1	1N751A	80131	04713
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU2	Socket, Integrated Circuit	1	ICN-246-S5-T	06776	
XU3*	Same as XU2				
XU4*	Socket, Integrated Circuit	2	ICN-183-S3-T	06776	
XU5*	Same as XU4				
XU6	Same as XU4				
XU7	Same as XU4				
XU9	Socket, Integrated Circuit	1	ICN-143-S3-T	06776	
XU16	Socket, Integrated Circuit	2	ICN-163-S3-T	06776	
XU17	Socket, Integrated Circuit	4	ICN-203-S3-T	06776	
XU18	Same as XU17				
XU19	Same as XU17				
XU20	Same as XU17				
XU21	Same as XU16				
Y1	Crystal: 4.91520 MHz	1	MP042	75378	
*	For Future Expansion				

6.5.2.1.2 Type 796046 Panel Interface/Demodulator Control REF DESIG PREFIX A2A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Electrolytic, Tantalum: 1.0 µF, 20%, 35 V	1	196D105X0035HE3	56289	
C2	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	4	196D186X9020KE3	56289	
C3	Same as C2				
C4	Same as C2				
C5	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	7	8131M100-651-104M	72982	
C6 Thru C11	Same as C5				
C12	Same as C2				
CR1	Diode	4	1N914/JAN	80131	93332
CR2	Same as CR1				
CR3	Same as CR1				
CR4	Same as CR1				
P1	Connector, Receptacle	1	65002-057	22526	
R1	Resistor, Fixed, Film: 1.33 kΩ, 1%, 1/10 W	1	RN55C1331F	81349	75042
R2	Resistor, Fixed, Film: 147 Ω, 1%, 1/10 W	1	RN55C1470F	81349	75042
R3	Resistor, Fixed, Film: 178 Ω, 1%, 1/10 W	1	RN55C1780F	81349	75042
R4	Resistor, Fixed, Film: 215 Ω, 1%, 1/10 W	2	RN55C2150F	81349	75042
R5	Same as R4				
R6	Resistor, Fixed, Film: 261 Ω, 1%, 1/10 W	1	RN55C2610F	81349	75042
R7	Resistor, Fixed, Film: 274 Ω, 1%, 1/10 W	1	RN55C2740F	81349	75042
R8	Resistor, Fixed, Film: 301 Ω, 1%, 1/10 W	1	RN55C3010F	81349	75042
R9	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100Ω/J	09021	
R10	Resistor, Variable, Film: 5 kΩ, 10%, 1/2 W	1	62PAR5K	73138	
R11	Resistor, Fixed, Film: 9.1 kΩ, 5%, 1/8 W	1	CF1/8-9.1kΩ/J	09021	
R12	Resistor, Fixed, Film: 15 Ω, 5%, 1/8 W	4	CF1/8-15Ω/J	09021	
R13	Same as R12				
R14	Same as R12				
R15	Same as R12				
R16	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47kΩ/J	09021	
U1	Integrated Circuit	1	SN74LS138N	01295	
U2	Integrated Circuit	2	P8282	34649	
U3	Same as U2				
U4	Integrated Circuit	1	P8155	34649	
U5	Integrated Circuit	2	LM324N	27014	
U6	Same as U5				
U7	Integrated Circuit	3	MC14490VP	04713	
U8	Same as U7				
U9	Same as U7				
U10	Integrated Circuit	2	SN74LS02N	01295	
U11	Integrated Circuit	1	AD7511DIKN	24355	

REF DESIG PREFIX A2A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U12	Same as U10				
U13	Integrated Circuit	1	DS3679N	27014	
U14	Integrated Circuit	1	SN74LS393N	01295	
XU2	Socket, Integrated Circuit	2	ICN-203-S3-T	06776	
XU3	Same as XU2				
XU4	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU14	Socket, Integrated Circuit	1	ICN-143-S3-T	06776	

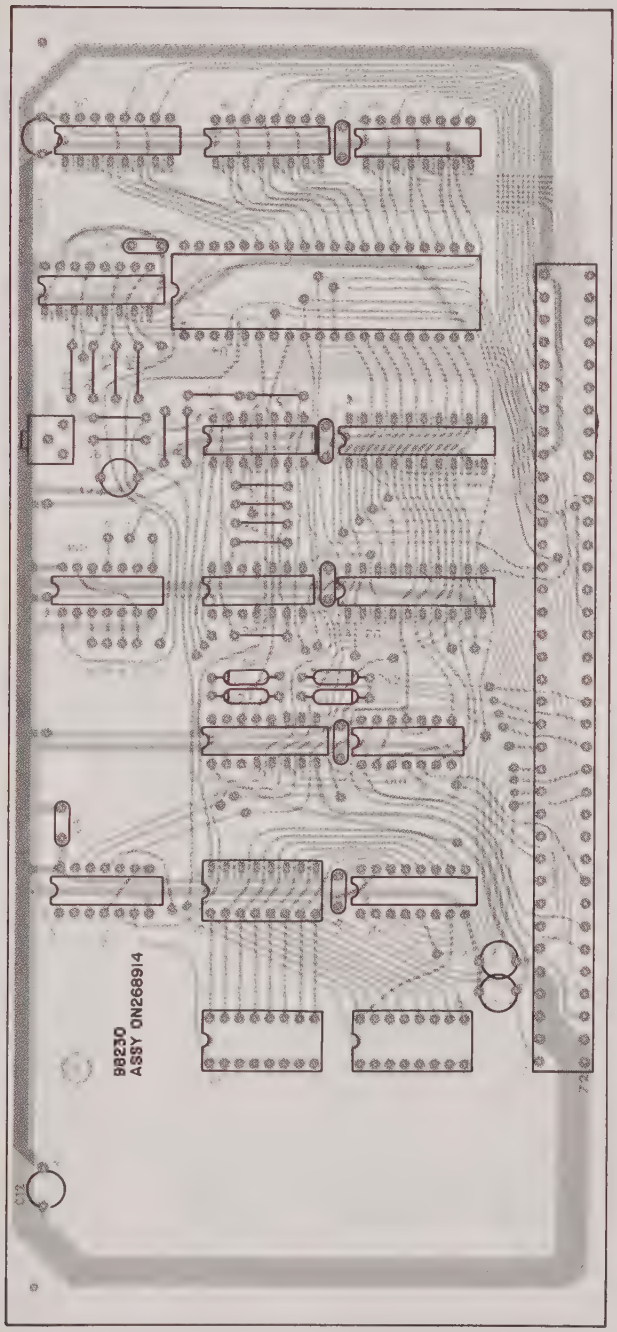


Figure 6-17. Type 796046 Panel Interface/Demodulator Control (A2A1A2), Location of Components

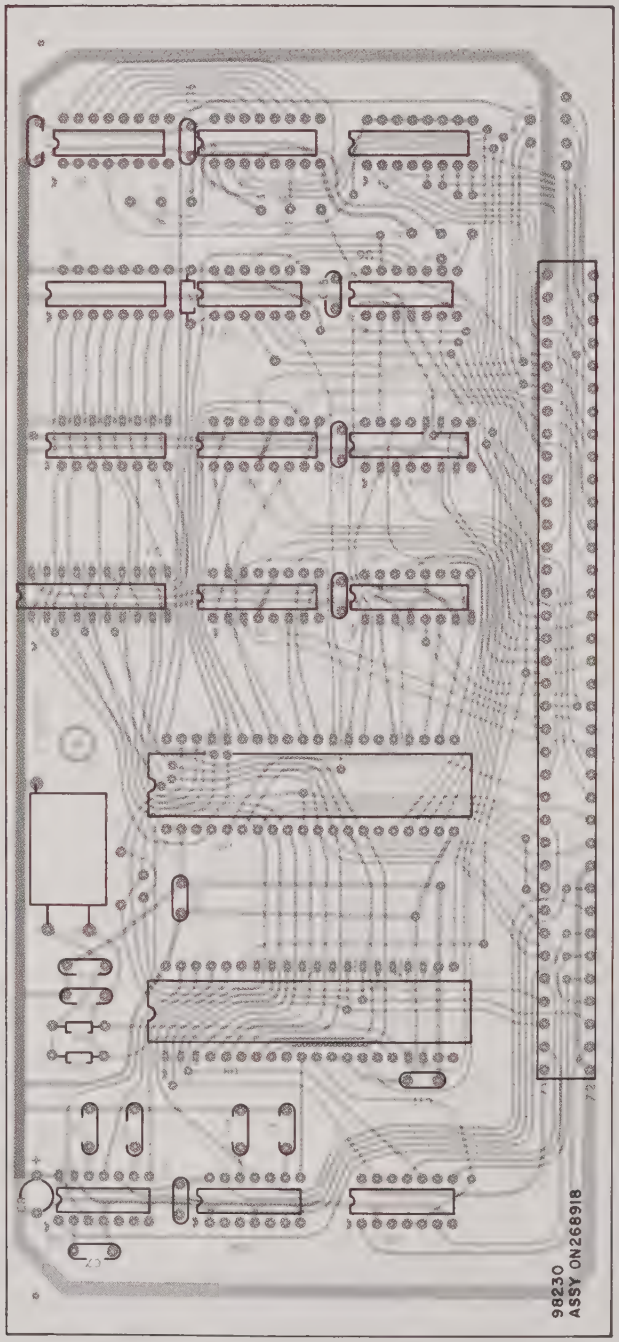


Figure 6-18. Type 796047-1 IEEE 488/RS-232 I/O Module (A2A1A3), Location of Components

6.5.2.1.3 Type 796047-1 IEEE 488/RS-232 I/O Module REF DESIG PREFIX A2A1A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Assembly Revision B				
C1 Thru C7	Not Used				
C8	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	1	196D186X9020KE3	56289	
C9	Capacitor, Ceramic, Disc: 0.1 µF, 10%, 100 V	5	8131M100-651-104M	72982	
C10	Not Used				
C11	Not Used				
C12	Not Used				
C13 Thru C16	Same as C9				
P1	Connector, Receptacle	1	65002-057	22526	
R1	Not Used				
R2	Not Used				
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10kΩ/J	09021	
S1	Not Used				
S2	Not Used				
S3	Switch, DIP	1	76PSB08	71450	
U1	Integrated Circuit	1	SN74LS138N	01295	
U2	Resistor, Network: 10 kΩ, 2%, 1/4 W	1	316B103	01121	
U3	Integrated Circuit	1	SN74LS244N	01295	
U4	Not Used				
U5	Integrated Circuit	1	SN74LS00N	01295	
U6	Integrated Circuit	1	SN74LS04N	01295	
U7	Integrated Circuit	1	MC68488P	04713	
U8	Not Used				
U9	Integrated Circuit	4	MC3448AP	04713	
U10	Same as U9				
U11	Same as U9				
U12	Same as U9				
U13	Not Used				
U14	Not Used				
XU3	Socket, Integrated Circuit	1	ICN-203-S3-T	06776	
XU7	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU8	Not Used				
XU9	Socket, Integrated Circuit	4	ICN-163-S3-T	06776	
XU10	Same as XU9				
XU11	Same as XU9				
XU12	Same as XU9				

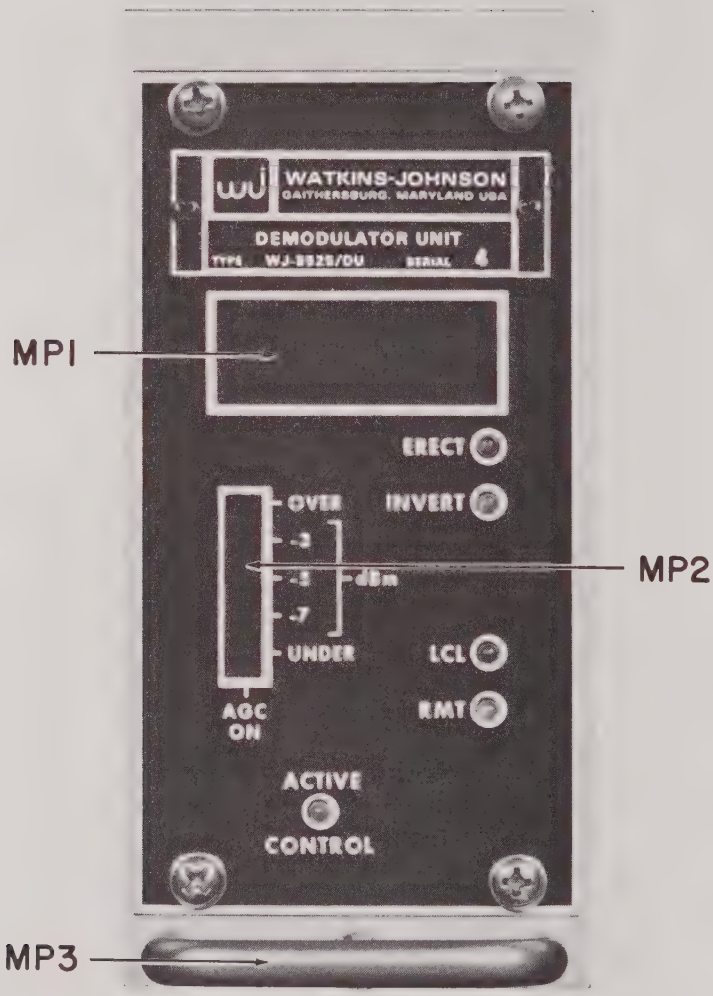


Figure 6-19. WJ-9525/DU Demodulator Unit (A3 thru A6), Front View, Location of Components

6.5.3 TYPE WJ-9525/DU DEMODULATOR UNIT REF DESIG PREFIX A3 Thru A6

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
A1	Motherboard, Demodulator Unit	1	796070	14632	
A2	Display	1	796067	14632	
A3	Display Driver	1	796068	14632	
FL1	Filter, Crystal: 2 MHz Delay Equalizer	1	92192	14632	
MP1	Display Window	1	280122-1	14632	
MP2	Display Window	1	280122-2	14632	
MP3	Handle, Front Panel	1	10227-B-0632-4A	06540	
MP4	Right Cover	1	480162	14632	
MP5	Left Cover	1	480161	14632	
	Accessory Items				
--	Extender Board	1	796089	14632	
--	Extender Board	1	796096	14632	

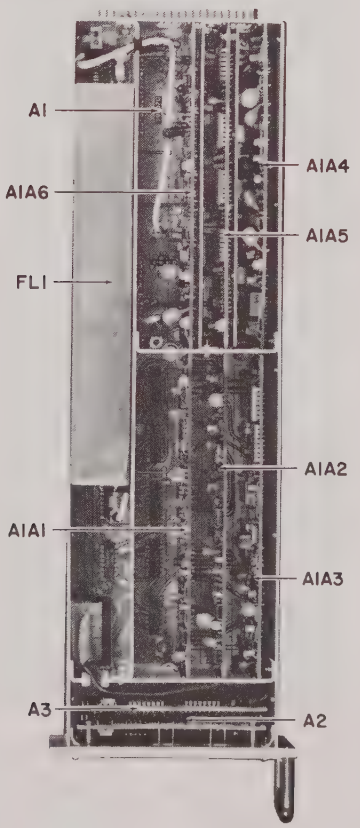


Figure 6-20. WJ-9525/DU Demodulator Unit (A3 thru A6), Right Side View, Location of Components

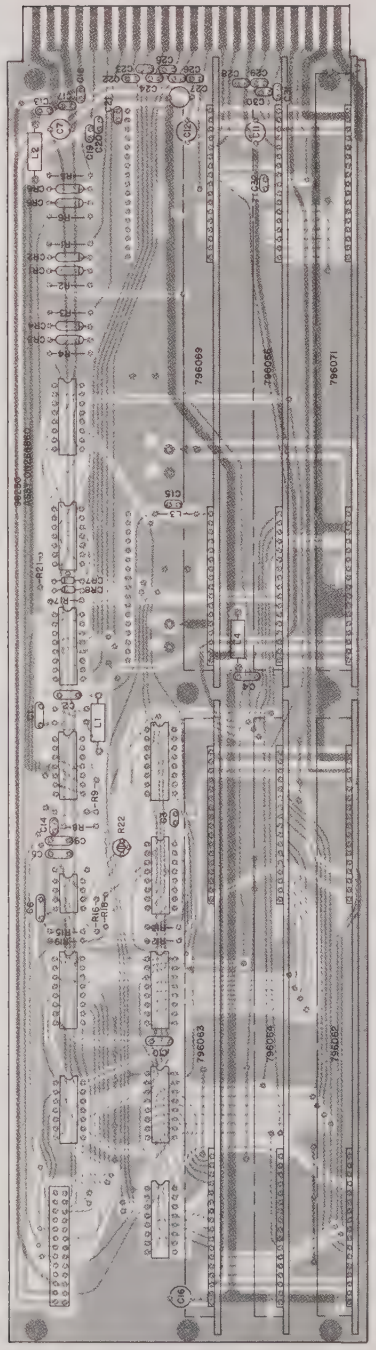


Figure 6-21. Type 796070 Motherboard, Demodulator Unit (A3A1 thru A6A1), Location of Components

6.5.3.1 Type 796070 Motherboard, Demodulator Unit REF DESIG PREFIX A3A1 Thru A6A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
A1	Fine Loop	1	796063	14632	
A2	Course Loop	1	796064	14632	
A3	Main Loop	1	796062	14632	
A4	Input Converter	1	796071	14632	
A5	Attenuator Control	1	796066	14632	
A6	IF Demodulator	1	796069	14632	
C1	Capacitor, Ceramic, Disc: 2200 pF, 5%, 50 V	2	8131-050C0G0-222J	72982	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 47 pF, 5%, 50 V	1	8111-050C0G0-470J	72982	
C4	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V	3	8131M100-651-474M	72982	
C5	Same as C4				
C6	Same as C4				
C7	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	4	196D186X9020KE3	56289	
C8	Same as C7				
C9	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	2	8131M100-651-104M	72982	
C10	Same as C9				
C11	Same as C7				
C12	Same as C7				
C13	Capacitor, Ceramic, Disc: 68 pF, 5%, 50 V	1	8121-050C0G0-680J	72982	
C14	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	8121-050-651-104M	72982	
C15	Capacitor, Ceramic, Disc: 6.8 pF, ±25 pF, 50 V	1	8101-050C0H0-689C	72982	
C16	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	1	196D107X0020TE4	56289	
C17	Capacitor, Ceramic, Disc: 1000 pF, 20%, 50 V	16	8101-050-651-102M	72982	
C18 Thru C32	Same as C17				
CR1	Diode	6	1N4444	80131	03508
CR2 Thru CR6	Same as CR1				
CR7	Diode	2	5082-2800	28480	
CR8	Same as CR7				
L1	Coil, Fixed: 6.8 µH	1	1025-40	99800	
L2	Coil, Fixed: 100 µH	1	1537-76	99800	
L3	Coil, Fixed: 10 µH	1	1025-44	99800	
L4	Coil, Fixed: 6.8 µH	1	1537-32	99800	
P1	Integral Part of Printed Wiring Board	X			
P2	Connector, Plug, SMA Series	1	521-3	16179	
P3	Connector, Plug, SMA Series	1	501-3	16179	
R1	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	3	CF1/8-47Ω/J	09021	
R2	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	3	CF1/8-1kΩ/J	09021	

REF DESIG PREFIX A3A1 Thru A6A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R3	Same as R1				
R4	Same as R2				
R5	Same as R1				
R6	Same as R2				
R7	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3kΩ/J	09021	
R8	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	2	CF1/8-1.5kΩ/J	09021	
R9	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470Ω/J	09021	
R10	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	1	CF1/8-220Ω/J	09021	
R11	Resistor, Fixed, Film: 62 Ω, 5%, 1/8 w	1	CF1/8-62Ω/J	09021	
R12	Resistor, Fixed, Film: 2.4 kΩ, 5%, 1/8 W	3	CF1/8-2.4kΩ/J	09021	
R13	Same as R12				
R14	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	3	CF1/8-100Ω/J	09021	
R15	Same as R14				
R16	Resistor, Fixed, Film: 1.3 kΩ, 5%, 1/8 W	1	CF1/8-1.3kΩ/J	09021	
R17	Same as R12				
R18	Resistor, Fixed, Film: 3 kΩ, 5%, 1/8 W	1	CF1/8-3kΩ/J	09021	
R19	Same as R8				
R20	Resistor, Fixed, Film: 51 Ω, 5%, 1/8 W	1	CF1/8-51Ω/J	09021	
R21	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10kΩ/J	09021	
R22	Resistor, Variable, Film: 1 kΩ, 10%, 1/2 W	1	62PR1K	73138	
U1	Integrated Circuit	1	MC14572UBCP	04713	
U2	Integrated Circuit	1	CD4093BE	02735	
U3	Integrated Circuit	1	MM74C175N	27014	
U4	Integrated Circuit	1	LM219D	27014	
U5	Integrated Circuit	1	MC1741SCP1	04713	
U6	Integrated Circuit	5	CD4094BE	02735	
U7	Integrated Circuit	1	SN74LS05N	01295	
U8	Same as U6				
U9	Integrated Circuit	1	MC1408L8	04713	
U10	Same as U6				
U11	Same as U6				
U12	Same as U6				
W1	Cable Assembly	1	380120-1	14632	
W2	Cable Assembly	1	380120-2	14632	
XA1P1	Socket, Connector, Receptacle	12	65500-117	22526	
XA1P2 Thru XA6P2	Same as XA1P1				

6.5.3.1.1 Type 796063 Fine Loop REF DESIG PREFIX A3A1A1 Thru A6A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	10	8121-050-651-104M	72982	
C2	Capacitor, Ceramic, Disc: 0.47 µF, 10%, 50 V	2	8131-050X7R0-474K	72982	
C3	Same as C2				
C4	Capacitor, Ceramic, Disc: 0.1 µF, 10%, 50 V	2	8121-050X7R0-104K	72982	
C5	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	4	196D186X9020KE3	56289	
C6	Same as C4				
C7	Same as C5				
C8	Capacitor, Ceramic, Disc: 330 pF, 10%, 50 V	8	8101-050X7R0-331K	72982	
C9	Same as C8				
C10	Capacitor, Ceramic, Disc: 4.7 pF, ±0.25 pF, 50 V	1	8101-050X7R0-479C	72982	
C11	Same as C8				
C12	Same as C5				
C13	Not Used				
C14	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C15	Capacitor, Ceramic, Disc: 4.3 pF, ±0.25 pF, 50 V	1	8101-050C0H0-439C	72982	
C16	Capaitor, Variable, Air: 0.8-10 pF, 250 V	1	5201	91293	
C17	Capacitor, Composition, Tubular: 0.51 pF, 10%, 500 V	1	QC0.51PFK	95121	
C18	Same as C8				
C19	Capacitor, Ceramic, Disc: 7.5 pF, ±0.25 pF, 50 V	1	8101-050C0H0-759C	72928	
C20	Same as C8				
C21	Same as C5				
C22	Same as C8				
C23	Same as C8				
C24	Same as C8				
C25 Thru C33	Same as C1				
C34	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	2	8121-050-651-103M	72982	
C35	Same as C34				
C36	Capacitor, Ceramic, Disc: 0.022 µF, 10%, 50 V	1	8111-050X7R0-223K	72982	
CR1	Diode	3	1N4449	80131	93332
CR2	Diode, Varicap	1	BB105B	25088	
CR3	Same as CR1				
CR4	Same as CR1				
CR5	Diode	1	5082-2800	28480	
L1	Coil, Fixed: 1.0 µH	3	1025-20	99800	
L2	Same as L1				
L3	Inductor	1	280131	14632	
L4	Same as L1				
MP1	Transipad	2	7717-44DAP	10103	
MP2	Same as MP1				

REF DESIG PREFIX A3A1A1 Thru A6A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				
Q1	Transistor	1	U310	17856	
Q2	Transistor	1	2N2857	80131	02735
R1	Resistor, Fixed, Film: 2 kΩ, 5%, 1/8 W	6	CF1/8-2kΩ/J	09021	
R2	Same as R1				
R3	Same as R1				
R4	Same as R1				
R5	Resistor, Fixed, Film: 56 kΩ, 5%, 1/8 W	2	CF1/8-56kΩ/J	09021	
R6	Same as R5				
R7	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	2	CF1/8-22Ω/J	09021	
R8	Same as R7				
R9	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	3	CF1/8-1kΩ/J	09021	
R10	Resistor, Fixed, Film: 91 kΩ, 5%, 1/8 W	1	CF1/8-91kΩ/J	09021	
R11	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	3	CF1/8-1.5kΩ/J	09021	
R12	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	1	CF1/8-10Ω/J	09021	
R13	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10kΩ/J	09021	
R14	Resistor, Fixed, Film: 11 kΩ, 5%, 1/8 W	1	CF1/8-11kΩ/J	09021	
R15	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22kΩ/J	09021	
R16	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	1	CF1/8-3.9kΩ/J	09021	
R17	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	2	CF1/8-47Ω/J	09021	
R18	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3kΩ/J	09021	
R19	Resistor, Fixed, film: 330 Ω, 5%, 1/8 W	1	CF1/8-330Ω/J	09021	
R20	Same as R17				
R21	Resistor, Fixed, Film: 110 Ω, 5%, 1/8 W	2	CF1/8-110Ω/J	09021	
R22	Resistor, Fixed, Film: 910 Ω, 5%, 1/8 W	2	CF1/8-910Ω/J	09021	
R23	Same as R9				
R24	Resistor, Fixed, Film: 470Ω, 5%, 1/8 W	2	CF1/8-47kΩ/J	09021	
R25	Same as R11				
R26	Same as R11				
R27	Same as R24				
R28	Same as R21				
R29	Same as R22				
R30	Same as R9				
R31	Resistor, Fixed, Film: 1.6 kΩ, 5%, 1/8 W	2	CF1/8-1.6kΩ/J	09021	
R32	Same as R31				
R33	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100Ω/J	09021	
R34	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47kΩ/J	09021	
R35	Resistor, Fixed, Film: 820 Ω, 5%, 1/8 W	1	CF1/8-820Ω/J	09021	
T1	Transformer	1	280132	14632	
U1	Integrated Circuit	1	11C44DC	07263	

REF DESIG PREFIX A3A1A1 Thru A6A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U2	Integrated Circuit	1	MC1741CP1	04713	
U3	Integrated Circuit	5	SN74LS669N	01295	
U4 Thru U7	Same as U3				
U8	Integrated Circuit	1	SN74LS168N	01295	
U9	Integrated Circuit	2	SP8647MDG	52648	
U10	Integrated Circuit	1	78L09AWC	07263	
U11	Same as U9				
U12	Integrated Circuit	1	SN74LS290N	01295	
U13	Integrated Circuit	1	SN74LS00N	01295	
VR1	Diode, Zener: 9.1 V	1	1N757A	80131	04713

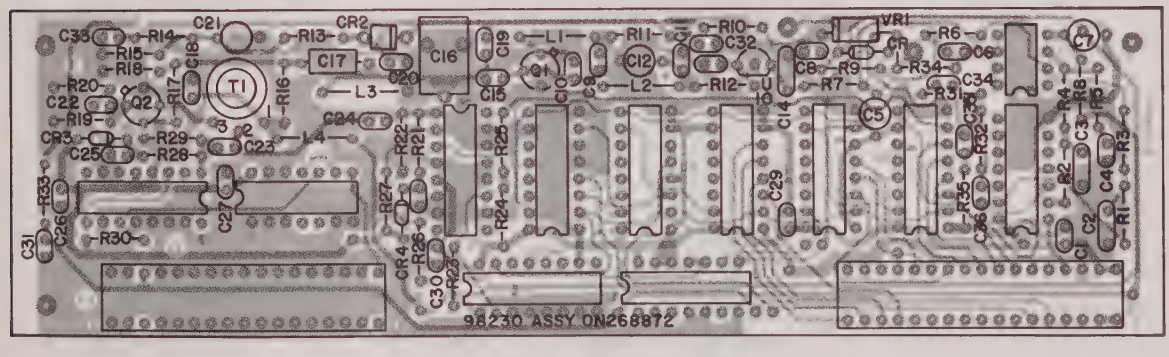


Figure 6-22. Type 796063 Fine Loop (A3A1A1 thru A6A1A1), Location of Components

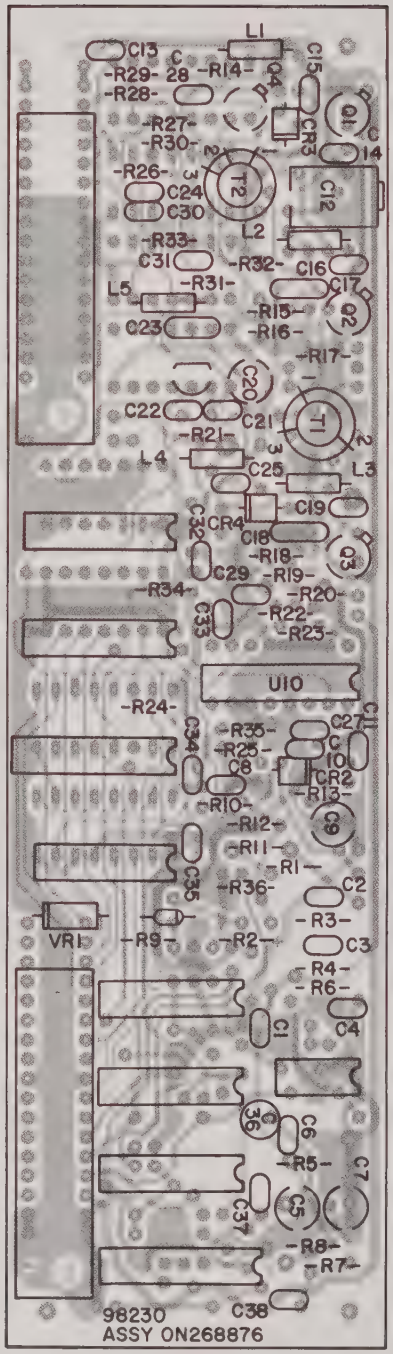


Figure 6-23. Type 796064 Coarse Loop (A3A1A2 thru A6A1A2), Location of Components

6.5.3.1.2 Type 796064 Coarse Loop REF DESIG PREFIX A3A1A2 Thru A6A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	8	8121-050-651-104M	72982	
C2	Capacitor, Ceramic, Disc: 4700 pF, 10%, 50 V	2	8121-050X7R0-472K	72982	
C3	Same as C2				
C4	Capacitor, Ceramic, Disc: 0.022 µF, 10%, 50 V	2	8111-050X7R0-233K	72982	
C5	Capacitor, Ceramic, Disc: 18 µF, 10%, 20 V	4	196D186X9020KE3	56289	
C6	Same as C4				
C7	Same as C5				
C8	Capacitor, Ceramic, Disc: 4700 pF, 20%, 50 V	12	8121-050-651-472M	72982	
C9	Same as C5				
C10	Same as C8				
C11	Capacitor, Ceramic, Disc: 68pF, 5%, 50V	2	8121-050-651-472J	72982	
C12	Capacitor, Variable, Air: 0.1-10 pF, 250 V	1	5201	91293	
C13	Same as C8				
C14	Same as C11				
C15	Capacitor, Ceramic, Disc: 10 pF, ±0.25 pF, 50 V	1	8101-050C0G0-100C	72982	
C16	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	3	34452-1	14632	
C17	Same as C8				
C18	Same as C16				
C19	Same as C8				
C20	Same as C5				
C21	Same as C8				
C22	Same as C1				
C23	Same as C16				
C24	Capacitor, Ceramic, Disc: 4.7 pF, ±0.25 pF, 50 V	1	8101-050C0H0-479C	72982	
C25	Same as C8				
C26	Not Used				
C27 Thru C31	Same as C8				
C32 Thru C35	Same as C1				
C36	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	1	196D107X0020TE4	56289	
C37	Same as C1				
C38	Same as C1				
CR1	Diode	1	1N4449	80131	93332
CR2	Diode, Varicap	1	BB109-YELLOW	25088	
CR3	Diode	2	MPN3401	04713	
CR4	Same as CR3				
L1	Coil, Fixed: 33 µH	3	1025-56	99800	

REF DESIG PREFIX A3A1A2 Thru A6A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
L2*	Coil, Fixed: 5.6 µH	1	1025-38	99800	
L3	Coil, Fixed: 3.9 µH	1	1025-34	99800	
L4	Same as L1				
L5	Same as L1				
MP1	Transipad	4	7717-44DAP	13103	
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				
Q1	Transistor	1	U310	17856	
Q2	Transistor	2	2N2222A	80131	04713
Q3	Same as Q2				
Q4	Transistor	1	2N2857	80131	04713
R1	Resistor, Fixed, Film: 1.8 kΩ, 5%, 1/8 W	4	CF1/8-1.8kΩ/J	09021	
R2	Same as R1				
R3	Same as R1				
R4	Same as R1				
R5	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/8 W	2	CF1/8-8.2kΩ/J	09021	
R6	Same as R5				
R7	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	2	CF1/8-22Ω/J	09021	
R8	Same as R7				
R9	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	2	CF1/8-3.9 kΩ/J	09021	
R10	Resistor, Fixed, Film: 91 kΩ, 5%, 1/8 W	1	CF1/8-91kΩ/J	09021	
R11	Resistor, Fixed, Film: 11 kΩ, 5%, 1/8 W	1	CF1/8-11kΩ/J	09021	
R12	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22kΩ/J	09021	
R13	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10kΩ/J	09021	
R14	Resistor, Fixed, Film: 3.6 kΩ, 5%, 1/8 W	2	CF1/8-3.6kΩ/J	09021	
R15	Same as R13				
R16	Resistor, Fixed, Film: 4.3 kΩ, 5%, 1/8 W	2	CF1/8-4.3kΩ/J	09021	
R17	Resistor, Fixed, Film: 1.1 kΩ, 5%, 1/8 W	2	CF1/8-1.1kΩ/J	09021	
R18	Same as R13				
R19	Same as R16				
R20	Same as R17				
R21	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	1	CF1/8-10Ω/J	09021	
R22	Resistor, Fixed, Film: 910 Ω, 5%, 1/8 W	1	CF1/8-910Ω/J	09021	
R23	Resistor, Fixed, Film: 68 kΩ, 5%, 1/8 W	1	CF1/8-68kΩ/J	09021	
R24	Same as R14				
R25	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	1	CF1/8-1.5kΩ/J	09021	
R26	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3kΩ/J	09021	
R27	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	1	CF1/8-820Ω/J	09021	
R28	Same as R27				
R29	Resistor, Fixed, Film: 820 Ω, 5%, 1/8 W	1	CF1/8-820Ω/J	09021	
*	Nominal Value, Final Value Factory Selected				

REF DESIG PREFIX A3A1A2 Thru A6A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R30	Same as R9				
R31	Resistor, Fixed, Film: 62 Ω, 5%, 1/8 W	2	CF1/8-62Ω/J	09021	
R32	Resistor, Fixed, Film: 200 Ω, 5%, 1/8 W	1	CF1/8-200Ω/J	09021	
R33	Same as R31				
R34	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	1	CF1/8-1kΩ/J	09021	
R35	Resistor, Fixed, Film: 2 kΩ, 5%, 1/8 W	1	CF1/8-2kΩ/J	09021	
R36	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47kΩ/J	09021	
T1	Transformer	1	280130-1	14632	
T2	Transformer	1	280133	14632	
U1	Integrated Circuit	1	SN74LS163AN	01295	
U2	Integrated Circuit	1	SN74LS00N	01295	
U3	Integrated Circuit	1	SN74LS290N	01295	
U4	Integrated Circuit	1	SN74LS113N	01295	
U5	Integrated Circuit	1	11C44DC	07263	
U6	Integrated Circuit	1	MC1741CP1	04713	
U7	Integrated Circuit	1	SN74LS190N	01295	
U8	Integrated Circuit	2	SN74LS669N	01295	
U9	Same as U8				
U10	Integrated Circuit	1	SP8690M	52648	
U11	Integrated Circuit	1	LM78L05ACZ	27014	
VR1	Diode, Zener: 9.1 V	1	1N757A	80131	04713

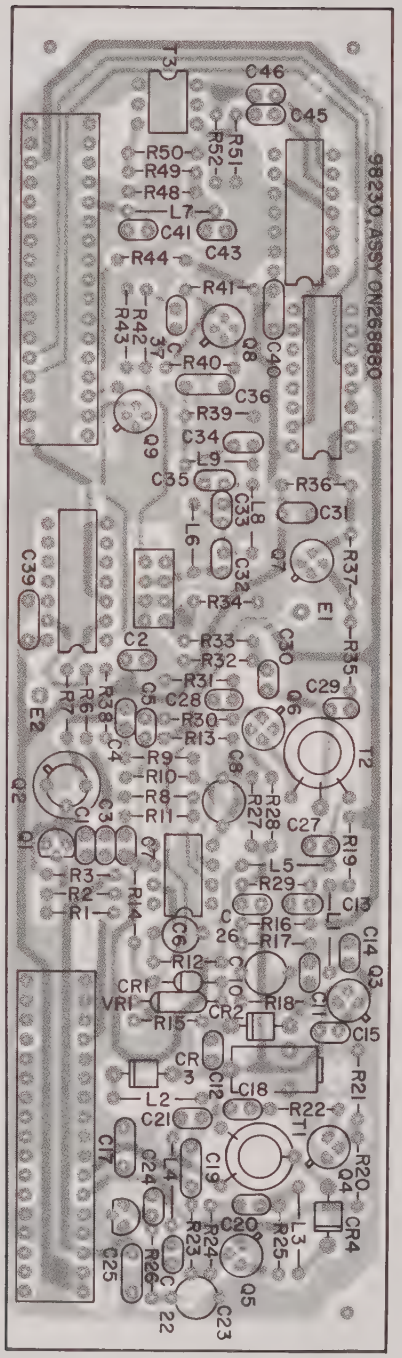


Figure 6-24. Type 796062 Main Loop (A3A1A3 thru A6A1A3), Location of Components

6.5.3.1.3 Type 796062 Main Loop REF DESIG PREFIX A3A1A3 Thru A6A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Ceramic, Disc: 0.022 µF, 10%, 50 V	1	8111-050X7R0-223K	72982	
C2	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	5	8121-050-651-104M	72982	
C3	Capacitor, Ceramic, Disc: 470 pF, 5%, 50 V	4	8121-050C0G0-471J	72982	
C4	Same as C3				
C5	Capacitor, Ceramic, Disc: 0.1 µF, 10%, 50 V	2	8121-050X7R0-104K	72982	
C6	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	4	196D186X9020KE3	56289	
C7	Same as C5				
C8	Same as C6				
C9	Not Used				
C10	Same as C6				
C11	Capacitor, Ceramic, Disc: 4700 pF, 20%, 50 V	10	8121-050-651-472M	72982	
C12	Capacitor, Mica, Dipped: 62 pF, 2%, 500V	1	CM04ED620G03	81349	
C13	Same as C11				
C14	Capacitor, Ceramic, Disc: 120 pf, 5%, 50 V	1	8121-050C0G0-121J	72982	
C15	Capacitor, Ceramic, Disc: 10 pF, ±0.25 pF, 50 V	1	8101-50C0G0-100C	72982	
C16	Capacitor, Variable, Air: 0.8-10 pF, 250 V	1	5201	91293	
C17	Capacitor, Ceramic, Disc: 0.47 µF, 10%, 50 V	3	8131-050X7R0-474K	72982	
C18	Same as C11				
C19	Same as C17				
C20	Same as C11				
C21	Same as C11				
C22	Same as C11				
C23	Same as C6				
C24	Same as C2				
C25	Same as C17				
C26	Capacitor, Ceramic, Disc: 4.7 pF, ±0.25 pF, 50 V	1	8101-050C0H0-479C	72982	
C27 Thru C30	Same as C11				
C31	Same as C2				
C32	Same as C3				
C33	Capacitor, Ceramic, Disc: 750 pF, 5%, 50 V	2	8121-050C0G0-751J	72982	
C34	Same as C3				
C35	Same as C33				
C36	Capacitor, Ceramic, Disc: 0.1µF, 20%, 100V	2	8131M100651-104M	72982	
C37	Capacitor, Ceramic, Disc: 68 pF, 5%, 50 V	1	8121-050C0G0-680J	72982	
C38	Not Used				
C39	Not Used				
C40	Same as C36				
C41	Capacitor, Ceramic, Disc: 1500 pF, 5%, 50 V	2	8131-050C0G0-152J	72982	
C42	Not Used				

REF DESIG PREFIX A3A1A3 Thru A6A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C43	Same as C41				
C44	Not Used				
C45	Same as C2				
C46	Same as C2				
CR1	Diode	1	1N4446	80131	93332
CR2	Diode, Varicap	1	BB109/YELLOW	25088	
CR3	Diode	2	MPN3401	04713	
CR4	Same as CR3				
L1	Coil, Fixed: 33 µH	3	1025-56	99800	
L2*	Coil, Fixed: 6.8 µH	1	1025-40	99800	
L3	Coil, Fixed: 3.3 µH	1	1025-32	99800	
L4	Same as L1				
L5	Same as L1				
L6	Coil, Fixed: 0.68 µH	2	1025-16	99800	
L7	Coil, Fixed: 3.9 µH	1	1025-34	99800	
L8	Coil, Fixed: 2.2 µH	1	1025-28	99800	
L9	Same as L6				
MP1	Transipad	7	7717-46DAP	13103	
MP2	Transipad	1	7717-44DAP	13103	
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				
Q1	Transistor	1	2N3904	80131	04713
Q2	Transistor	1	2N2386	80131	01295
Q3	Transistor	1	U310	17856	
Q4	Transistor	2	2N2222A	80131	04713
Q5	Same as Q4				
Q6	Transistor	4	2N2857	80131	02735
Q7	Same as Q6				
Q8	Same as Q6				
Q9	Same as Q6				
R1	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	2	CF1/8-3.3kΩ/J	09021	
R2	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	6	CF1/8-10kΩ/J	09021	
R3	Resistor, Fixed, Film: 2.2MΩ, 5%, 1/8 W	1	CF1/8-2.2MΩ/J	09021	
R4	Not Used				
R5	Not Used				
R6	Resistor, Fixed, Film: 1.6 kΩ, 5%, 1/8 W	4	CF1/8-1.6kΩ/J	09021	
R7	Same as R6				
R8	Same as R6				
R9	Same as R6				
*	Nominal Value, Final Value Factory Selected				

REF DESIG PREFIX A3A1A3 Thru A6A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R10	Resistor, Fixed, Film: 390 Ω, 5%, 1/8 W	2	CF1/8-390Ω/J	09021	
R11	Same as R10				
R12	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	3	CF1/8-22Ω/J	09021	
R13	Same as R12				
R14	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	2	CF1/8-3.9kΩ/J	09021	
R15	Resistor, Fixed, Film: 91 kΩ, 5%, 1/8 W	1	CF1/8-91kΩ/J	09021	
R16	Resistor, Fixed, Film: 11 kΩ, 5%, 1/8 W	1	CF1/8-11kΩ/J	09021	
R17	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22kΩ/J	09021	
R18	Same as R2				
R19	Resistor, Fixed, Film: 3.6 kΩ, 5%, 1/8 W	1	CF1/8-3.6kΩ/J	09021	
R20	Same as R2				
R21	Resistor, Fixed, Film: 4.3 kΩ, 5%, 1/8 W	2	CF1/8-4.3kΩ/J	09021	
R22	Resistor, Fixed, Film: 1.1 kΩ, 5%, 1/8 W	2	CF1/8-1.1kΩ/J	09021	
R23	Same as R2				
R24	Same as R21				
R25	Same as R22				
R26	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	2	CF1/8-10Ω/J	09021	
R27	Same as R1				
R28	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	1	CF1/8-47Ω,J	09021	
R29	Same as R14				
R30	Resistor, Fixed, Film: 330 Ω, 5%, 1/8 W	2	CF1/8-330Ω/J	09021	
R31	Same as R26				
R32	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	2	CF1/8-220Ω/J	09021	
R33	Same as R12				
R34	Same as R32				
R35	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	4	CF1/8-1kΩ/J	09021	
R36	Same as R30				
R37	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/8 W	1	CF1/8-6.8kΩ/J	09021	
R38	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47kΩ/J	09021	
R39	Resistor, Fixed, Film: 51 Ω, 5%, 1/8 W	1	CF1/8-51Ω/J	09021	
R40	Resistor, Fixed, Film: 27 kΩ, 5%, 1/8 W	1	CF1/8-27kΩ/J	09021	
R41	Same as R35				
R42	Same as R2				
R43	Same as R2				
R44	Resistor, Fixed, Film: 750 Ω, 5%, 1/8 W	1	CF1/8-750Ω/J	09021	
R45	Not Used				
R46	Not Used				
R47	Not Used				
R48	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	2	CF1/8-100Ω/J	09021	
R49	Resistor, Fixed, Film: 68 Ω, 5%, 1/8 W	1	CF1/8-68Ω/J	09021	
R50	Same as R48				

REF DESIG PREFIX A3A1A3 Thru A6A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R51	Same as R35				
R52	Same as R35				
T1	Coil, Toroidal	1	280130-2	14632	
T2	Transformer	1	280133	14632	
T3	Transformer	1	T9-1	15542	
U1	Integrated Circuit	1	11C44DC	07263	
U2	Integrated Circuit	1	MC1741CP1	04713	
U3	Not Used				
U4	Integrated Circuit	1	SN74LS169N	01295	
U5	Integrated Circuit	1	SN74LS113N	01295	
U6	Mixer	1	TSM-1	15542	
U7	Not Used				
U8	Integrated Circuit	1	LM78L05ACZ	27014	
VR1	Diode, Zener: 9.1 V	1	1N757A	80131	04713

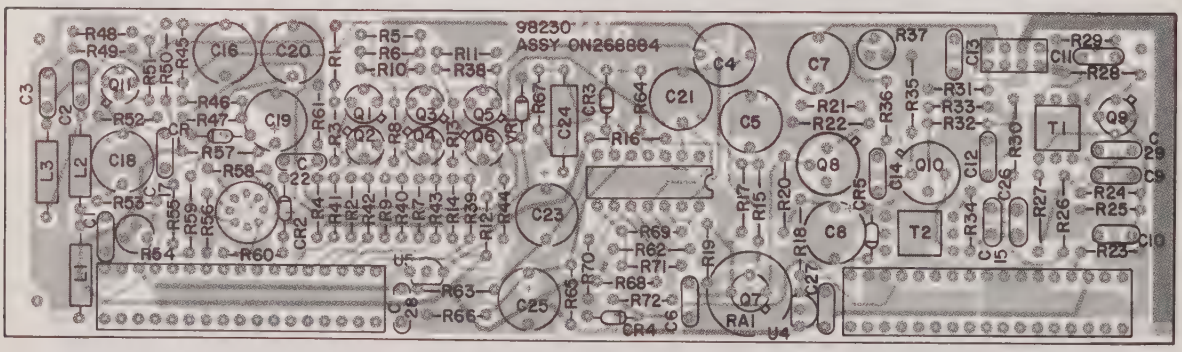


Figure 6-25. Type 796071 Input Converter/Attenuator (A3A1A4 thru A6A1A4), Location of Components

6.5.3.1.4 Type 796071 Input Converter/Attenuator REF DESIG PREFIX A3A1A4 Thru A6A1A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision B				
C1	Capacitor, Ceramic, Disc: 6800 pF, 5%, 50 V	2	8131-050C0G0-682J	72982	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V	4	8131M100651-474M	72982	
C4	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	5	196D107X0020TE4	56289	
C5	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	5	196D476X0020PE4	56289	
C6	Same as C3				
C7	Same as C4				
C8	Same as C4				
C9	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	8	8131M100651-104M	72982	
C10 Thru C14	Same as C9				
C15	Capacitor, Mica, Dipped: 100 pF, 2%, 500 V	1	CM04FD101G03	81349	72136
C16	Same as C4				
C17	Capacitor, Ceramic, Disc: 0.47 µF, 10%, 100 V	1	CK06BX473K	81349	56289
C18	Same as C4				
C19	Same as C5				
C20	Same as C5				
C21	Same as C5				
C22	Same as C9				
C23	Same as C5				
C24	Capacitor, Electrolytic, Tantalum: 4.7 µF, 10%, 35 V	1	CS13BF475K	81349	56289
C25	Capacitor, Electrolytic, Tantalum: 1.0 µF, 20%, 25 V	1	196D105X0035HE3	56289	
C26*	Capacitor, Mica, Dipped: 100 pF, 2%, 500 V	1	CM04FD101G03	81349	72136
C27	Same as C3				
C28	Same as C3				
C29	Same as C9				
CR1	Diode	2	1N4446	80131	93332
CR2	Diode	3	5082-2800	28480	
CR3	Same as CR2				
CR4	Same as CR1				
CR5	Same as CR2				
FB1	Ferrite, Bead	9	P5-1288	01037	
FB2 Thru FB9	Same as FB1				
L1	Coil, Fixed: 15 µH	2	1537-40	99800	
L2	Coil, Fixed: 33 µH	1	1537-52	99800	
L3	Same as L1				
	*Nominal Value, Final Value Factory Selected				

REF DESIG PREFIX A3A1A4 Thru A6A1A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
MP1	Transipad (Q1-Q6)	7	7717-16DAP	13103	
MP2	Transipad (Q7)	1	7717-115DAP	13103	
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				
Q1	Transistor	6	2N4445	80131	04713
Q2 Thru Q6	Same as Q1				
Q7	Transistor	1	CP643	12498	
Q8	Transistor	1	2N2270	80131	02735
Q9	Transistor	1	2N2857	80131	02735
Q10	Transistor	1	2N5109	80131	02735
Q11	Transistor	1	841001-1	14632	
R1	Resistor, Fixed, Film: 16 Ω, 5%, 1/8 W	4	CF1/8-16Ω/J	09021	
R2	Resistor, Fixed, Film: Composition: 6.8 MΩ, 5%, 1/8 W	6	RCR05G685JS	81349	01121
R3	Resistor, Fixed, Film: 56 Ω, 5%, 1/8 W	2	CF1/8-56Ω/J	09021	
R4	Same as R2				
R5	Same as R1				
R6	Same as R1				
R7	Same as R2				
R8	Same as R3				
R9	Same as R2				
R10	Same as R1				
R11	Resistor, Fixed, Film: 30 Ω, 5%, 1/8 W	2	CF1/8-30Ω/J	09021	
R12	Same as R2				
R13	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	1	CF1/8-18Ω/J	09021	
R14	Same as R2				
R15	Resistor, Fixed, Composition: 910 Ω, 5%, 1/4 W	1	RCR07G911JS	81349	01121
R16	Resistor, Fixed, Composition: 47 Ω, 5%, 1/4 W	2	RCR07G470JS	81349	01121
R17	Resistor, Fixed, Composition: 1 MΩ, 5%, 1/8 W	1	RCR05G105JS	81349	01121
R18	Resistor, Fixed, Composition: 22 Ω, 5%, 1/4 W	1	RCR07G220JS	81349	01121
R19	Resistor, Fixed, Composition: 680 kΩ, 5%, 1/8 W	1	RCR05G684JS	81349	01121
R20	Resistor, Fixed, Composition: 330 Ω, 5%, 1/4 W	3	RCR07G331JS	81349	01121
R21	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	2	CF1/8-47Ω/J	09021	
R22	Resistor, Fixed, Composition: 470 Ω, 5%, 1/4 W	1	RCR07G471JS	81349	01121
R23	Resistor, Fixed, Film: 51 Ω, 5%, 1/8 W	2	CF1/8-51Ω/JS	09021	
R24	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	1	CF1/8-12kΩ/J	09021	
R25	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/8 W	2	CF1/8-6.8kΩ/J	09021	
R26	Same as R16				
R27	Resistor, Fixed, Film: 430 Ω, 5%, 1/8 W	1	CF1/8-430Ω/J	09021	
R28	Same as R20				
R29	Resistor, Fixed, Film: 33 Ω, 5%, 1/8 W	1	CF1/8-33Ω/J	09021	

REF DESIG PREFIX A3A1A4 Thru A6A1A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R30	Resistor, Fixed, Composition: 100 Ω, 5%, 1/4 W	6	RCR07G101JS	81349	01121
R31	Same as R23				
R32	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	2	CF1/8-4.7kΩ/J	09021	
R33	Same as R25				
R34	Resistor, Fixed, Film: 750 Ω, 5%, 1/8 W	1	CF1/8-750Ω/J	09021	
R35	Same as R20				
R36	Resistor, Fixed, Film: 12 Ω, 5%, 1/8 W	1	CF1/8-12Ω/J	09021	
R37	Resistor, Variable, Film: 50 Ω, 10%, 1/2 W	1	62PR50	73138	
R38	Same as R11				
R39	Resistor, Fixed, Film: 200 kΩ, 5%, 1/8 W	6	CF1/8-200kΩ/J	09021	
R40 Thru R44	Same as R39				
R45	Resistor, Fixed, Film: 120 kΩ, 5%, 1/8 W	1	CF1/8-120kΩ/J	09021	
R46	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	2	CF1/8-33kΩ/J	09021	
R47	Resistor, Fixed, Film: 39 kΩ, 5%, 1/8 W	1	CF1/8-39kΩ/J	09021	
R48	Resistor, Fixed, Film: 150 kΩ, 5%, 1/8 W	1	CF1/8-150kΩ/J	09021	
R49	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10kΩ/J	09021	
R50	Same as R30				
R51	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	1	CF1/8-1.5kΩ/J	09021	
R52	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	1	CF1/8-270Ω/J	09021	
R53	Same as R21				
R54	Resistor, Variable, Film: 200 Ω, 10%, 1/2 W	1	62PR200	73138	
R55	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	2	CF1/8-15kΩ/J	09021	
R56	Same as R55				
R57	Same as R30				
R58	Resistor, Fixed, Film: 910kΩ, 5%, 1/8 W	1	CF1/8-910kΩ/J	09021	
R59	Same as R30				
R60	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470Ω/J	09021	
R61	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100kΩ/J	09021	
R62	Same as R30				
R63	Same as R30				
R64	Resistor, Fixed, Film: 2.0 kΩ, 5%, 1/8 W	1	CF1/8-2kΩ/J	09021	
R65	Resistor, Fixed, Film: 20 kΩ, 5%, 1/8 W	1	CF1/8-20kΩ/J	09021	
R66	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/8 W	1	CF1/8-2.7kΩ/J	09021	
R67	Resistor, Fixed, Composition: 20 MΩ, 5%, 1/8 W	1	RCR05G206JS	81349	01121
R68	Same as R46				
R69	Same as R49				
R70	Same as R32				
R71	Same as R49				
R72	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	1	CF1/8-1.0kΩ/J	09021	
RA1	Heatsink	1	2220B	13103	

REF DESIG PREFIX A3A1A4 Thru A6A1A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
T1	Transformer	2	T9-1	15542	
T2	Same as T1				
U1	Mixer	1	TXM-1	15542	
U2	Integrated Circuit	1	CA3100T	02735	
U3	Integrated Circuit	1	RC4136DB	49956	
U4	Voltage Regulator	1	MC78L12ACP	04713	
U5	Integrated Circuit	1	LM79L12ACZ	27014	
VR1	Diode, Zener: 8.2 V	1	1N756A	80131	04713

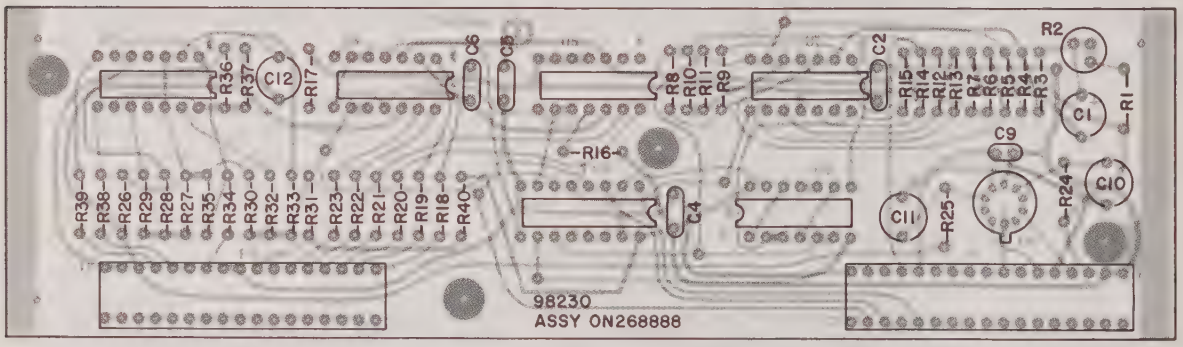


Figure 6-26. Type 796066 Attenuator Control (A3A1A5 thru A6A1A5), Location of Components

6.5.3.1.5 Type 796066 Attenuator Control REF DESIG PREFIX A3A1A5 Thru A6A1A5

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	1	196D105X0035HE3	56289	
C2	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	4	34452-1	72982	
C3	Not Used				
C4	Same as C2				
C5	Same as C2				
C6	Same as C2				
C7	Not Used				
C8	Not Used				
C9	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	8121-050-651-104M	72982	
C10	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	3	196D186X9020KE3	56289	
C11	Same as C10				
C12	Same as C10				
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				
R1	Resistor, Fixed, Film: 9.1 kΩ, 5%, 1/8 W	1	CF1/8-9.1kΩ/J	09021	
R2	Resistor, Variable, Film: 2 kΩ, 10%, 1/2 W	1	62PAR2K	73138	
R3	Resistor, Fixed, Film: 910 Ω, 5%, 1/8 W	1	CF1/8-910Ω/J	09021	
R4	Resistor, Fixed, Film: 360 Ω 5%, 1/8 W	1	CF1/8-360Ω/J	09021	
R5	Resistor, Fixed, Film: 240 Ω, 5%, 1/8 W	2	CF1/8-240Ω/J	09021	
R6	Same as R5				
R7	Resistor, Fixed, Film: 2.4 kΩ, 5%, 1/8 W	1	CF1/8-2.4kΩ/J	09021	
R8	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10kΩ/J	09021	
R9	Resistor, Fixed, Film: 270 kΩ, 5%, 1/8 W	4	CF1/8-270kΩ/J	09021	
R10	Same as R8				
R11	Same as R9				
R12	Same as R8				
R13	Same as R9				
R14	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15kΩ/J	09021	
R15	Same as R9				
R16	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3kΩ/J	09021	
R17	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	1	CF1/8-1.5kΩ/J	09021	
R18	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	8	CF1/8-1.0kΩ/J	09021	
R19 Thru R23	Same as R18				
R24	Resistor, Fixed, Film: 100 Ω 5%, 1/8 W	3	CF1/8-100Ω/J	09021	
R25	Same as R24				
R26	Same as R24				
R27	Resistor, Fixed, Film: 1.8 kΩ, 5%, 1/8 W	1	CF1/8-1.8kΩ/J	09021	
R28	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	2	CF1/8-270Ω/J	09021	
R29	Same as R28				

REF DESIG PREFIX A3A1A5 Thru A6A1A5

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R30	Same as R18				
R31	Resistor, Fixed, Film: 27 kΩ, 5%, 1/8 W	1	CF1/8-27kΩ/J	09021	
R32	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	2	CF1/8-47Ω/J	09021	
R33	Same as R32				
R34	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	2	CF1/8-47k/J	09021	
R35	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	2	CF1/8-100kΩ/J	09021	
R36	Same as R35				
R37	Same as R34				
R38	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	2	CF1/8-10Ω/J	09021	
R39	Same as R38				
R40	Same as R18				
U1	Integrated Circuit	1	LM324N	27014	
U2	Integrated Circuit	1	SN74LS02N	01295	
U3	Integrated Circuit	1	SN74LS157N	01295	
U4	Integrated Circuit	2	LM239N	27014	
U5	Same as U4				
U6	Integrated Circuit	1	DG188BA	32292	
U7	Integrated Circuit	1	MPQ2484	04713	

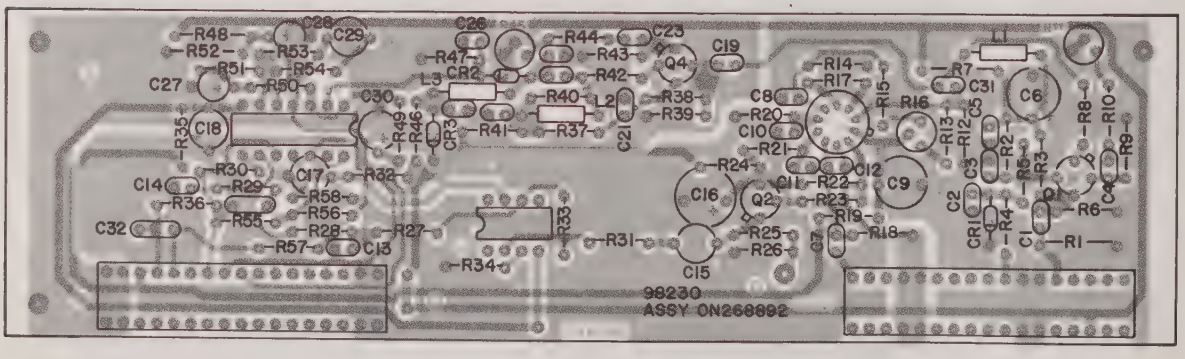


Figure 6-27. Type 796069 IF Demodulator (A3A1A6 thru A6A1A6), Location of Components

6.5.3.1.6 Type 796069 IF Demodulator REF DESIG PREFIX A3A1A6 Thru A6A1A6

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision C				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	14	8121-050-651-104M	72982	
C2 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	3	196D107X0020TE3	56289	
C7	Same as C1				
C8	Same as C1				
C9	Same as C6				
C10	Same as C1				
C11	Capacitor, Ceramic, Disc: 1000 pF, 5%, 50 V	1	8121-050C0G0-102J	72982	
C12	Capacitor, Ceramic, Disc: 470 pF, 5%, 50 V	1	8121-050C0G0-471J	72982	
C13	Capacitor, Ceramic, Disc: 1800 pF, 5%, 50 V	1	8121-050C0G0-182J	72982	
C14	Capacitor, Ceramic, Disc: 130 pF, 5%, 50 V	1	8121-050C0G0-131J	72982	
C15	Capacitor, Electrolytic, Tantalum: 10 µF, 20%, 20 V	1	196D106X0020JE3	56289	
C16	Same as C6				
C17	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	2	196D186X9020KE3	56289	
C18	Same as C17				
C19	Capacitor, Ceramic, Disc: 10 pF, ±0.25 pF, 50 V	1	8101-050C0G0-100C	72982	
C20 Thru C23	Same as C1				
C24	Capacitor, Ceramic, Disc: 18 pF, 5%, 50 V	1	8101-050C0G0-180J	72982	
C25	Same as C1				
C26	Capacitor, Ceramic, Disc: 27 pF, 5%, 50 V	1	8111-050C0G0-270J	72982	
C27	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	2	196D105X0035HE3	56289	
C28	Same as C27				
C29	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
C30	Capacitor, Electrolytic, Tantalum: 27 µF, 10%, 35 V	1	196D276X9035TE4	56289	
C31	Same as C1				
C32	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 200 V	1	8131A200Z5U103M	72982	
C33	Capacitor, Ceramic, Disc: 6800 pF, 5%, 50 V	1	8131-050C0G0-682J	72982	
CR1	Diode	1	1N4444	80131	03508
CR2	Diode	3	5082-2800	28480	
CR3	Same as CR2				
CR4	Same as CR2				
L1	Coil, Fixed: 270 µH	1	1025-78	99800	
L2	Coil, Fixed: 470 µH	2	2025-84	99800	
L3	Same as L2				
MP1	Transipad	3	7717-44DAP	13103	
P1	Connector, Plug	2	65001-020	22526	
P2	Same as P1				

REF DESIG PREFIX A3A1A6 Thru A6A1A6

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
Q1	Transistor	2	841001-1	14632	
Q2	Transistor	1	2N2222A	80131	04713
Q3	Not Used				
Q4	Same as Q1				
R1	Resistor, Fixed, Film: 51.1 Ω, 1%, 1/4 W	1	CC51R1F	01121	
R2	Resistor, Fixed, Film: 120 kΩ, 5%, 1/8 W	2	CF1/8-120kΩ/J	09021	
R3	Resistor, Fixed, Film: 150 kΩ, 5%, 1/8 W	2	CF1/8-150kΩ/J	09021	
R4	Resistor, Fixed, Film: 18 kΩ, 5%, 1/8 W	1	CF1/8-18kΩ/J	09021	
R5	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	2	CF1/8-33kΩ/J	09021	
R6	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	2	CF1/8-10kΩ/J	09021	
R7	Resistor, Fixed, Film: 220 Ω, 5%, 1/4 W	1	CF1/8-220Ω/J	09021	
R8	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	2	CF1/8-10Ω/J	09021	
R9	Resistor, Fixed, Film: 150 Ω 5%, 1/8 W	1	CF1/8-150Ω/J	09021	
R10	Resistor, Fixed, Film: 15 Ω, 5%, 1/8 W	1	CF1/8-15Ω/J	09021	
R11	Resistor, Variable, Film: 200 Ω, 10%, 1/2 W	2	62PR200	73138	
R12	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	5	CF1/8-15kΩ/J	09021	
R13	Same as R12				
R14	Same as R12				
R15	Same as R12				
R16	Resistor, Variable, Film: 2 kΩ, 10%, 1/2 W	1	62PR2K	73138	
R17	Resistor, Fixed, Film: 1.2 kΩ, 5%, 1/8 W	1	CF1/8-1.2kΩ/J	09021	
R18	Resistor, Fixed, Film: 51 Ω, 5%, 1/8 W	2	CF1/8-51Ω/J	09021	
R19	Resistor, Fixed, Film: 2.4 kΩ, 5%, 1/8 W	1	CF1/8-2.4kΩ/J	09021	
R20	Resistor, Fixed, Film: 9.1 kΩ, 5%, 1/8 W	1	CF1/8-9.1kΩ/J	09021	
R21	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	2	CF1/8-3.9kΩ/J	09021	
R22	Same as R21				
R23	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	1	CF1/8-47Ω/J	09021	
R24	Resistor, Fixed, Film: 1 kΩ, 5%, 1/8 W	4	CF1/8-1kΩ/J	09021	
R25	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/8 W	3	CF1/8-6.8kΩ/J	09021	
R26	Same as R18				
R27	Resistor, Fixed, Film: 27 kΩ, 5%, 1/8 W	3	CF1/8-27kΩ/J	09021	
R28	Same as R27				
R29	Same as R27				
R30	Resistor, Fixed, Film: 82kΩ, 5%, 1/8 W	1	CF1/8-82kΩ/J	09021	
R31	Same as R35				
R32	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	3	CF1/8-100Ω/J	09021	
R33	Same as R5				
R34	Same as R25				
R35	Same as R32				
R36	Resistor, Fixed, Film: 300 Ω, 5%, 1/8 W	2	CF1/8-300Ω/J	09021	
R37	Same as R2				

REF DESIG PREFIX A3A1A6 Thru A6A1A6

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R38	Resistor, Fixed, Film: 24 kΩ, 5%, 1/8 W	1	CF1/8-24kΩ/J	09021	
R39	Same as R6				
R40	Same as R12				
R41	Same as R32				
R42	Same as R8				
R43	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	1	CF1/8-270Ω/J	09021	
R44	Resistor, Fixed, Film: 27 Ω, 5%, 1/8 W	1	CF1/8-27Ω/J	09021	
R45	Same as R11				
R46	Same as R3				
R47	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100kΩ/J	09021	
R48	Resistor, Fixed, Film: 7.5 kΩ, 1%, 1/4 W	1	CC7501F	01121	
R49	Same as R24				
R50	Same as R24				
R51	Same as R24				
R52	Resistor, Fixed, Film: 1 kΩ, 1%, 1/4 W	1	CC1001F	01121	
R53	Resistor Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47kΩ/J	09021	
R54	Resistor, Fixed, Film: 1.8 kΩ, 1%, 1/8 W	1	CF1/8-1.8kΩ/J	09021	
R55	Resistor, Fixed, Film: 2.2 kΩ, 1%, 1/8 W	2	CF1/8-2.2kΩ/J	09021	
R56	Same as R55				
R57	Same as R56				
R58	Resistor, Fixed, Film: 1.1 kΩ, 5%, 1/8 W	1	CF1/8-1.1kΩ/J	09021	
T1	Transformer	1	LL010	07388	
U1	Integrated Circuit	1	MC1596G	04713	
U2	Integrated Circuit	1	RC4136DB	49956	
U3	Integrated Circuit	1	MC1741CP1	04713	

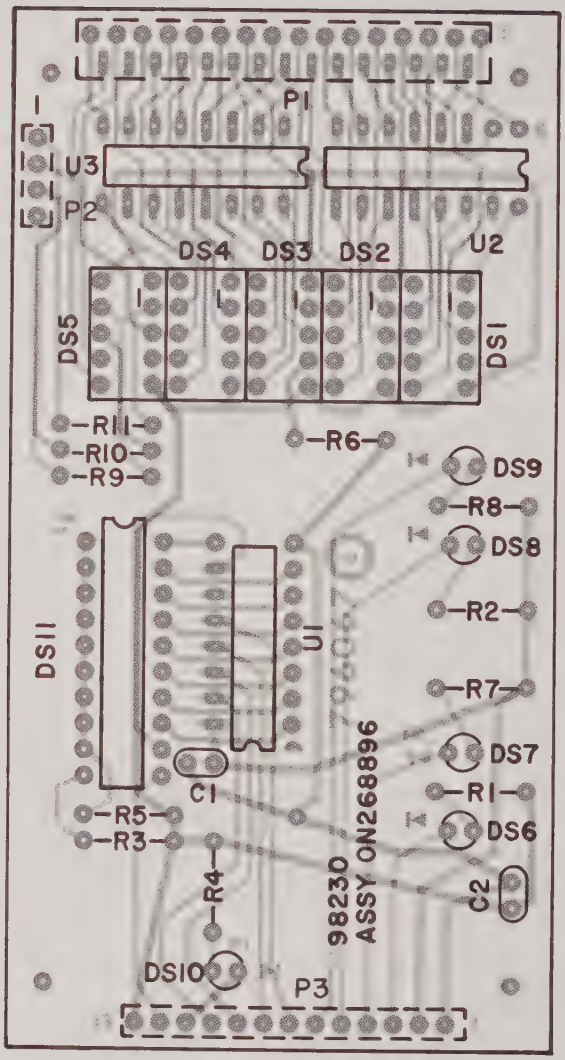


Figure 6-28. Type 796067 Display Board (A3A2 thru A6A2), Location of Components

6.5.3.2 Type 796067 Display Board REF DESIG PREFIX A3A2 thru A6A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
	Assembly Revision A				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	8121-050-651-104M	72982	
C2	Same as C1				
DS1	Display, LED Numeric (Red)	5	FND360	07263	
DS2 Thru DS5	Same as DS1				
DS6	Diode, LED (Yellow)	3	5082-4584	28480	
DS7	Diode, LED (Green)	2	5082-4984	28480	
DS8	Same as DS6				
DS9	Same as DS7				
DS10	Same as DS6				
DS11	Display, LED	1	RBG-1000	50579	
P1A	Terminal Strip	1	TS-116-G-AA	55322	
P1B	Terminal Strip	1	TS-115-G-AA	55322	
P2	Terminal Strip	1	TS-104-G-AA	55322	
P3	Terminal Strip	1	TS-113-G-AA	55322	
R1	Resistor, Fixed, Film: 390 Ω, 5%, 1/8 W	8	CF1/8-390Ω/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	3	CF1/8-470Ω/J	09021	
R4	Same as R1				
R5	Same as R3				
R6	Same as R3				
R7 Thru R11	Same as R1				
U1	Integrated Circuit	1	SN74LS145N	01295	
U2	Resistor, Network: 390 Ω	2	898-3-R390	73138	
U3	Same as U2				
XDS1	Socket, Connector, Receptacle	10	SS105G-2	55322	
XDS2 Thru XDS5	Same as XDS1				
XDS6 Thru XDS10	Not Used				
XDS11	Socket, Integrated Circuit	1	CA-20S-10SD	52072	

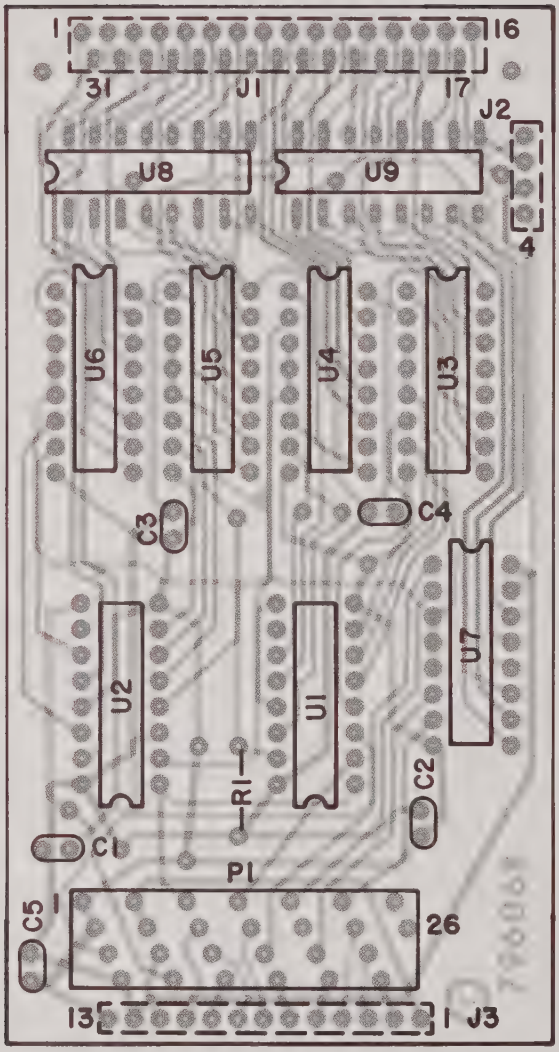


Figure 6-29. Type 796068 Display Driver (A3A3 thru A6A3), Location of Components

6.5.3.2.1 Type 796068 Display Driver REF DESIG PREFIX A3A3 Thru A6A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Assembly Revision A				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	5	8121-050-651-104M	72982	
C2 Thru C5	Same as C1				
J1A	Connector, Receptacle	1	SS-116-G-2	55322	
J1B	Connector, Receptacle	1	SS-115-G-2	55322	
J2	Connector, Receptacle	1	SS-104-G-2	55322	
J3	Connector, Receptacle	1	SS-113-G-2		
--	Cable Assembly	1	380123	14632	
MP1	Connector, Paddleboard	1	88216-5	00779	
P1	Connector, Plug Kit	1	88476-5	00779	
R1	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470 Ω/J	09021	
U1	Integrated Circuit	2	CD4094BE	02735	
U2	Same as U1				
U3	Integrated Circuit	5	SN74LS47N	01295	
U4 Thru U7	Same as U3				
U8	Resistor, Network: 390 Ω, 2%, 1/4 W	2	898-3-R390	73138	
U9	Same as U8				

SECTION VII
SCHEMATIC DIAGRAMS

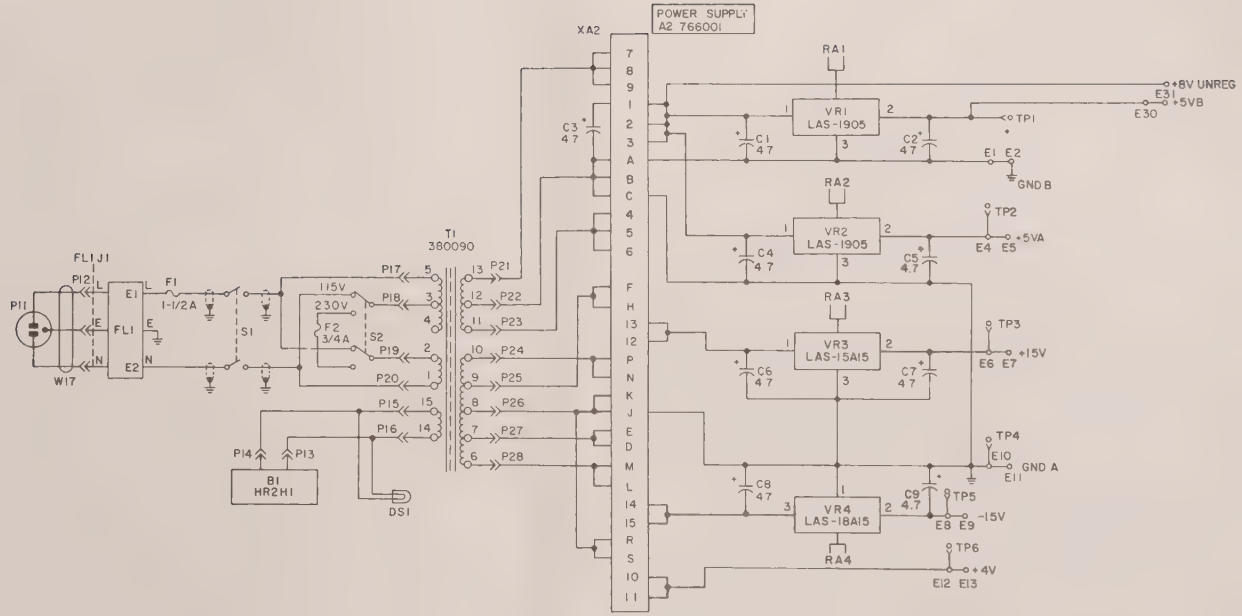


Figure 7-1. WJ-9525/CRF Control Rack Frame (A1), Schematic Diagram (Sheet 1 of 3)

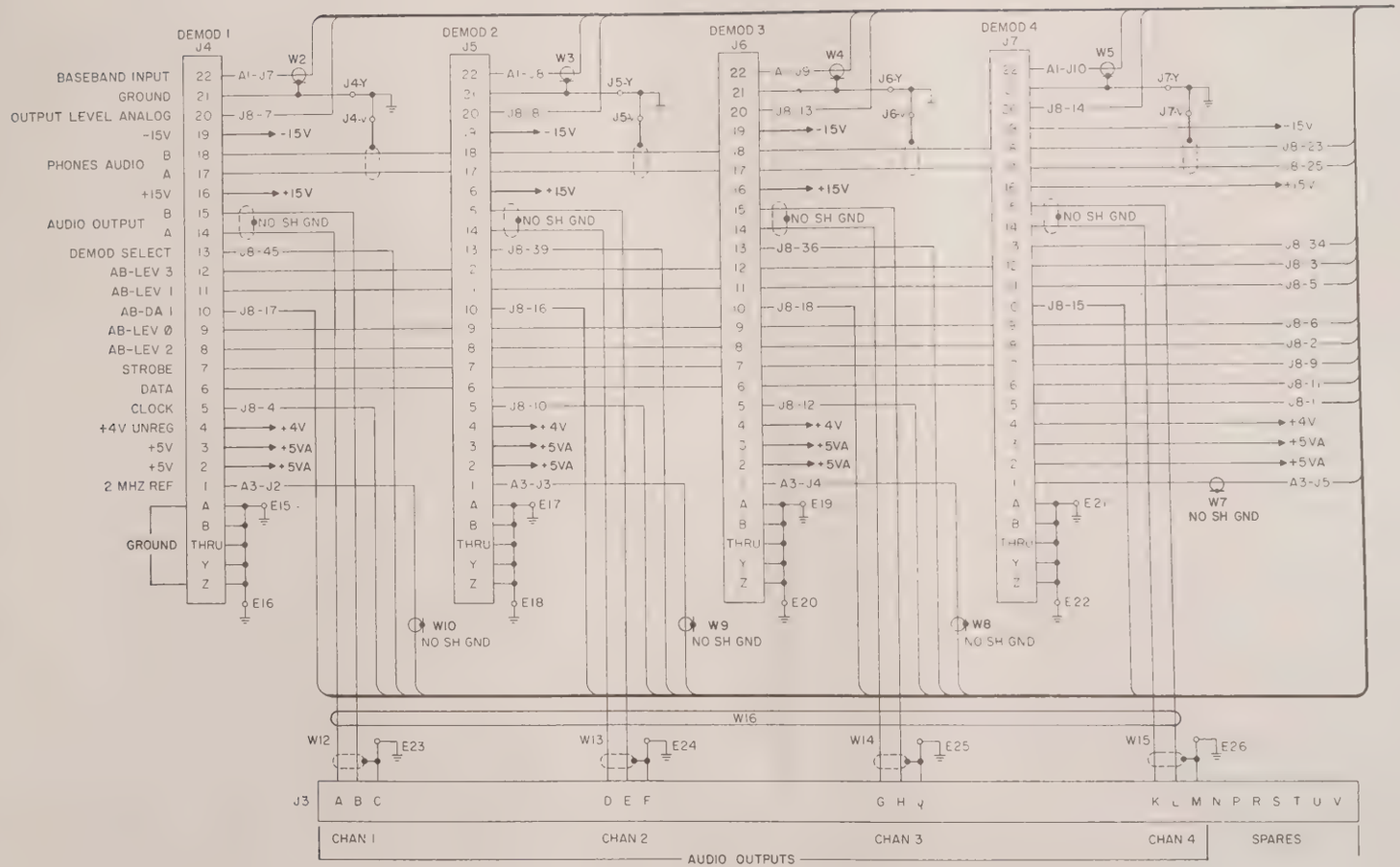


Figure 7-1. WJ-9525/CRF Control Rack Frame (A1), Schematic Diagram (Sheet 2 of 3)

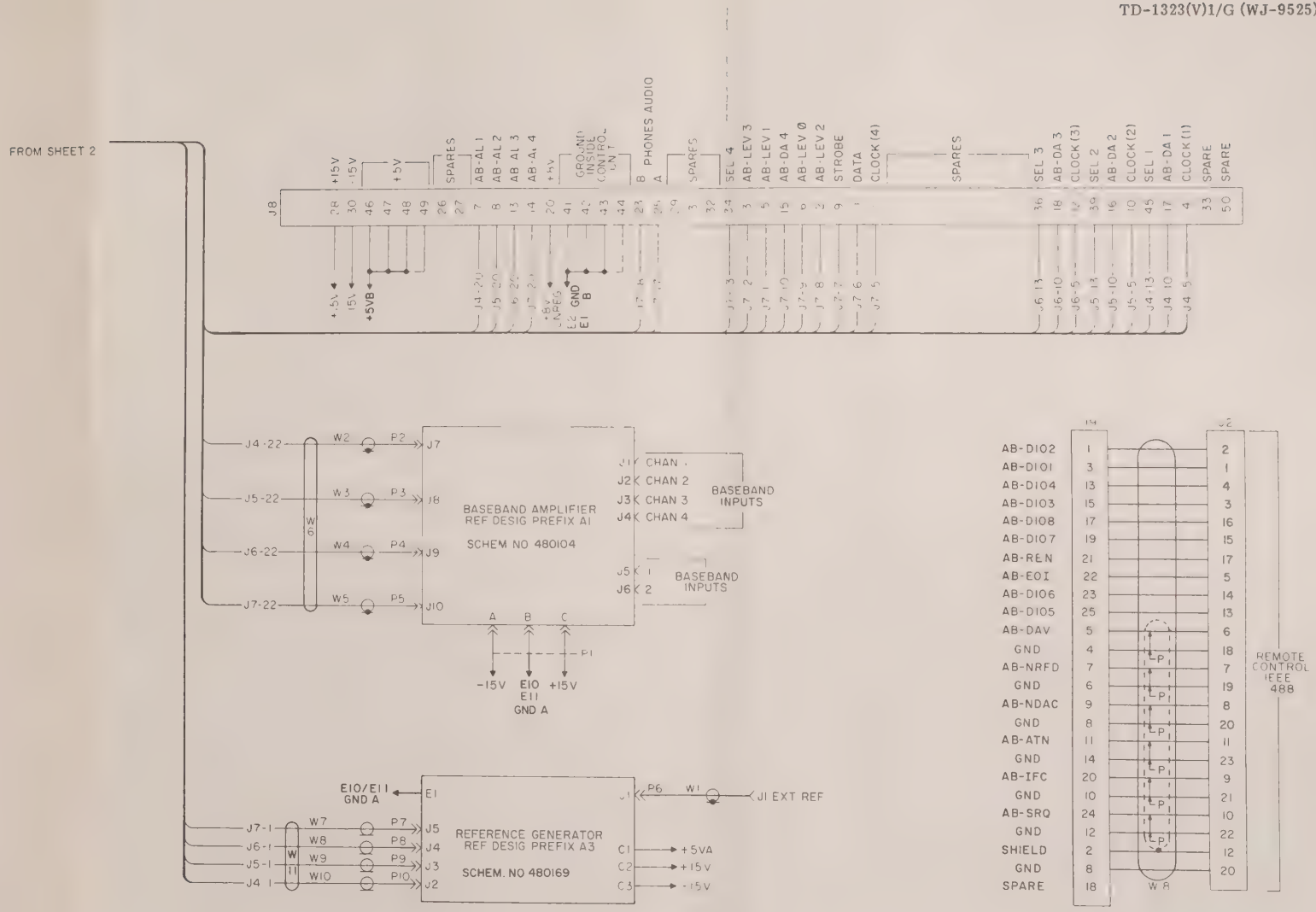
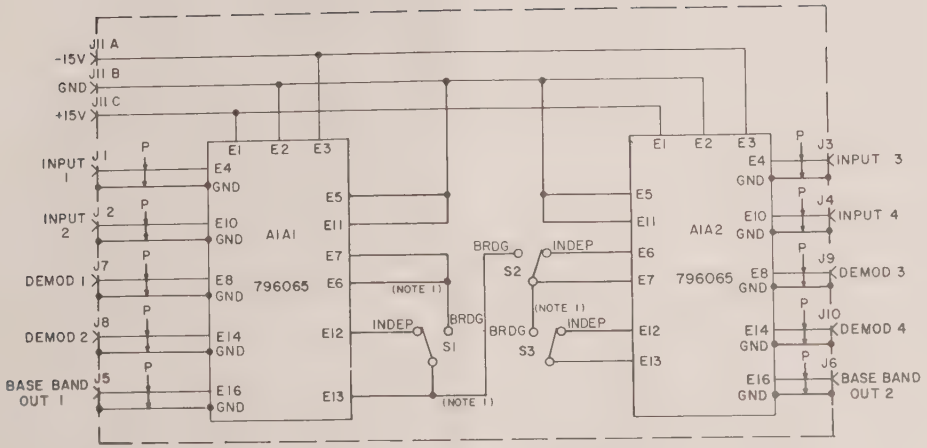


Figure 7-1. WJ-9525/CRF Control Rack Frame (A1), Schematic Diagram (Sheet 3 of 3)



NOTE:
1. #24 WIRE SHORT AS POSSIBLE.

Figure 7-2. Type 796074 Baseband Signal Distribution Amplifier (A1A1), Schematic Diagram

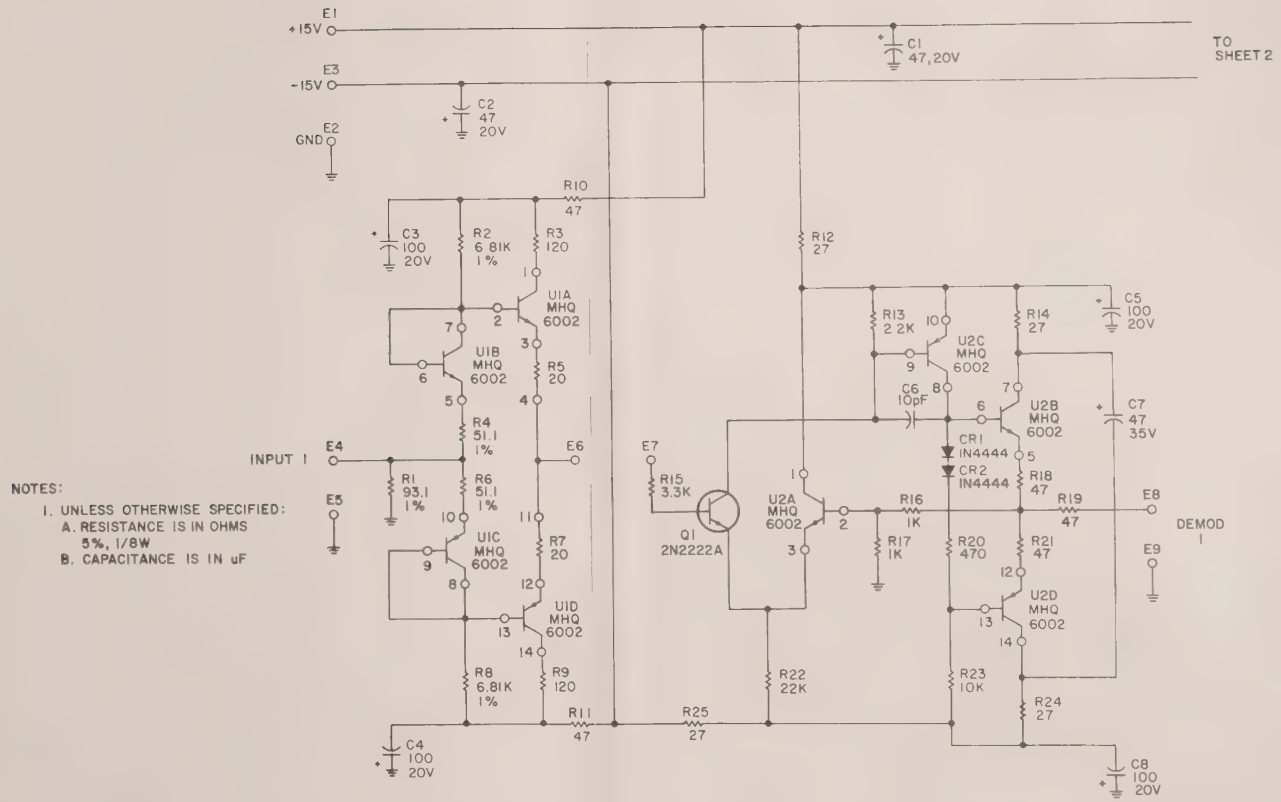


Figure 7-3. Type 796065 Baseband Signal Distribution Amplifier PC Assembly (A1A1A1, A1A1A2), Schematic Diagram (Sheet 1 of 2)

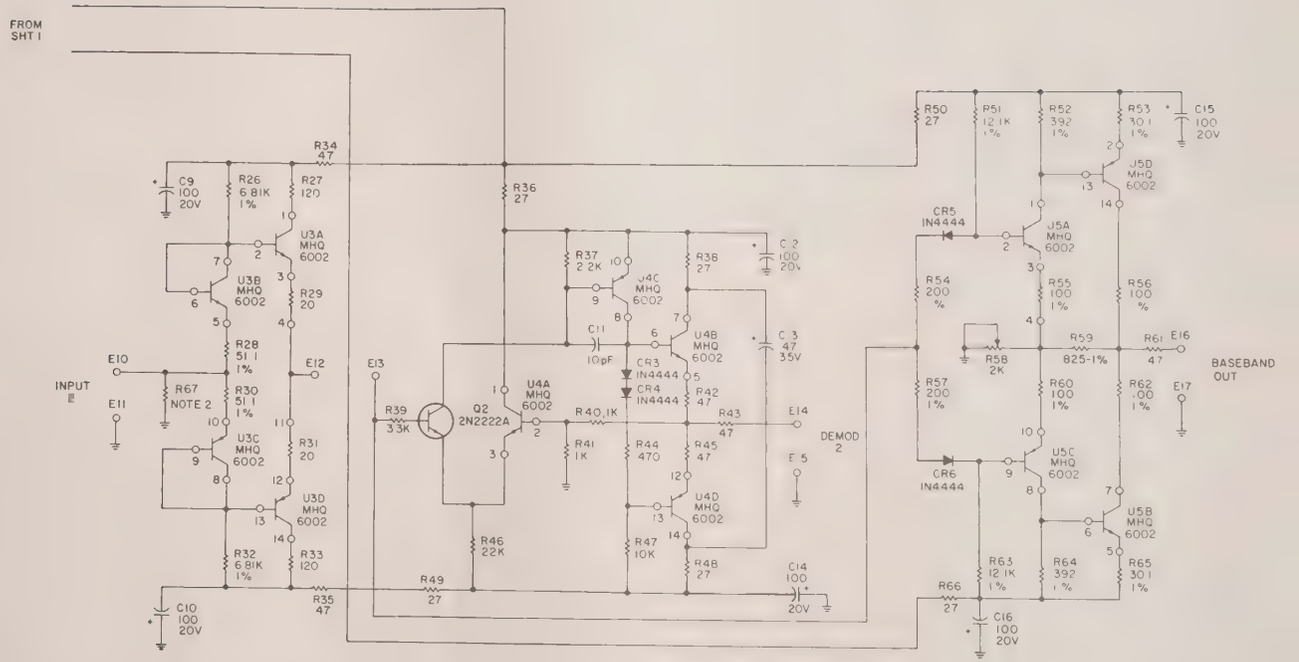


Figure 7-3. Type 796065 Baseband Signal Distribution Amplifier PC Assembly (A1A1A1, A1A1A2), Schematic Diagram (Sheet 2 of 2)

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE ARE IN OHMS ±5%, 1/4W
2. ALL CAPACITANCE IS IN μF

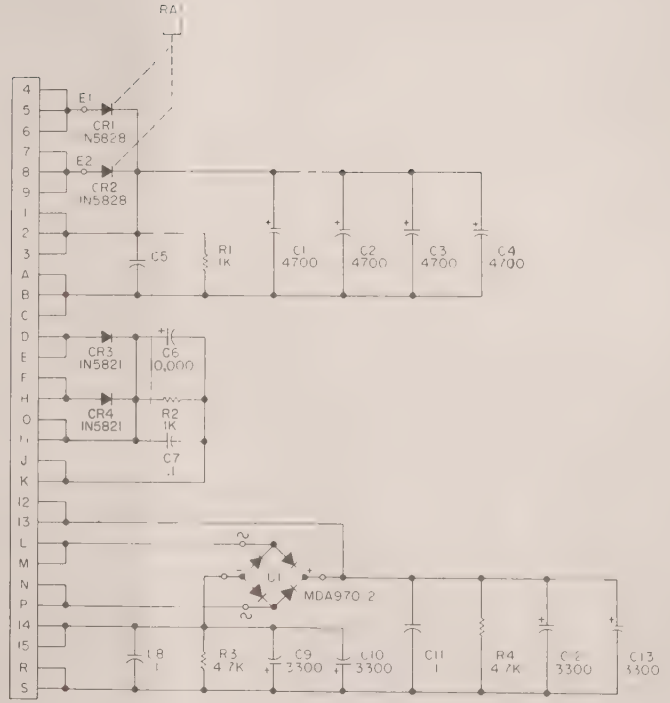


Figure 7-4. Type 766001 Power Supply (A1A2), Schematic Diagram

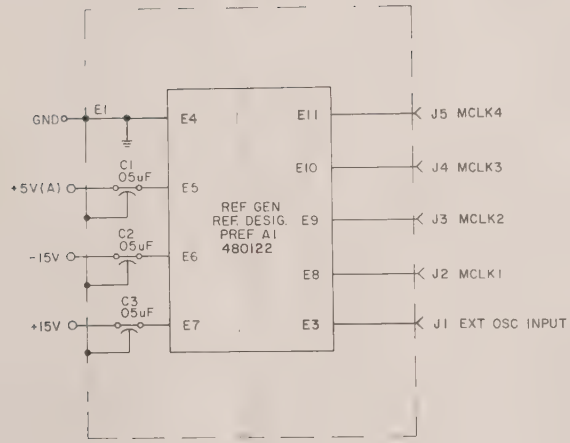
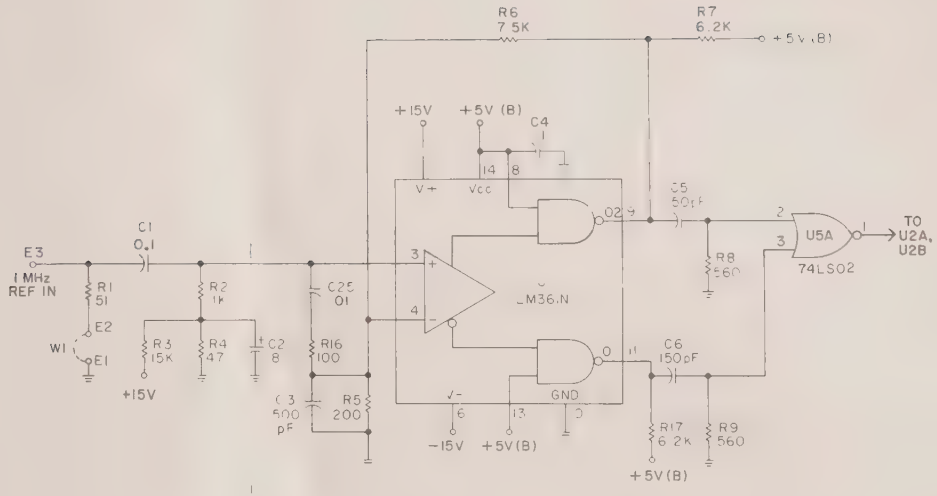


Figure 7-5. Type 796060 Reference Generator (A1A3), Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   A. RESISTANCE IS IN OHMS ±5%, 1/8W
   B. CAPACITANCE IS IN uF

Figure 7-6. Part 380084 Reference Generator PC Assembly (A1A3A1), Schematic Diagram (Sheet 1 of 2)

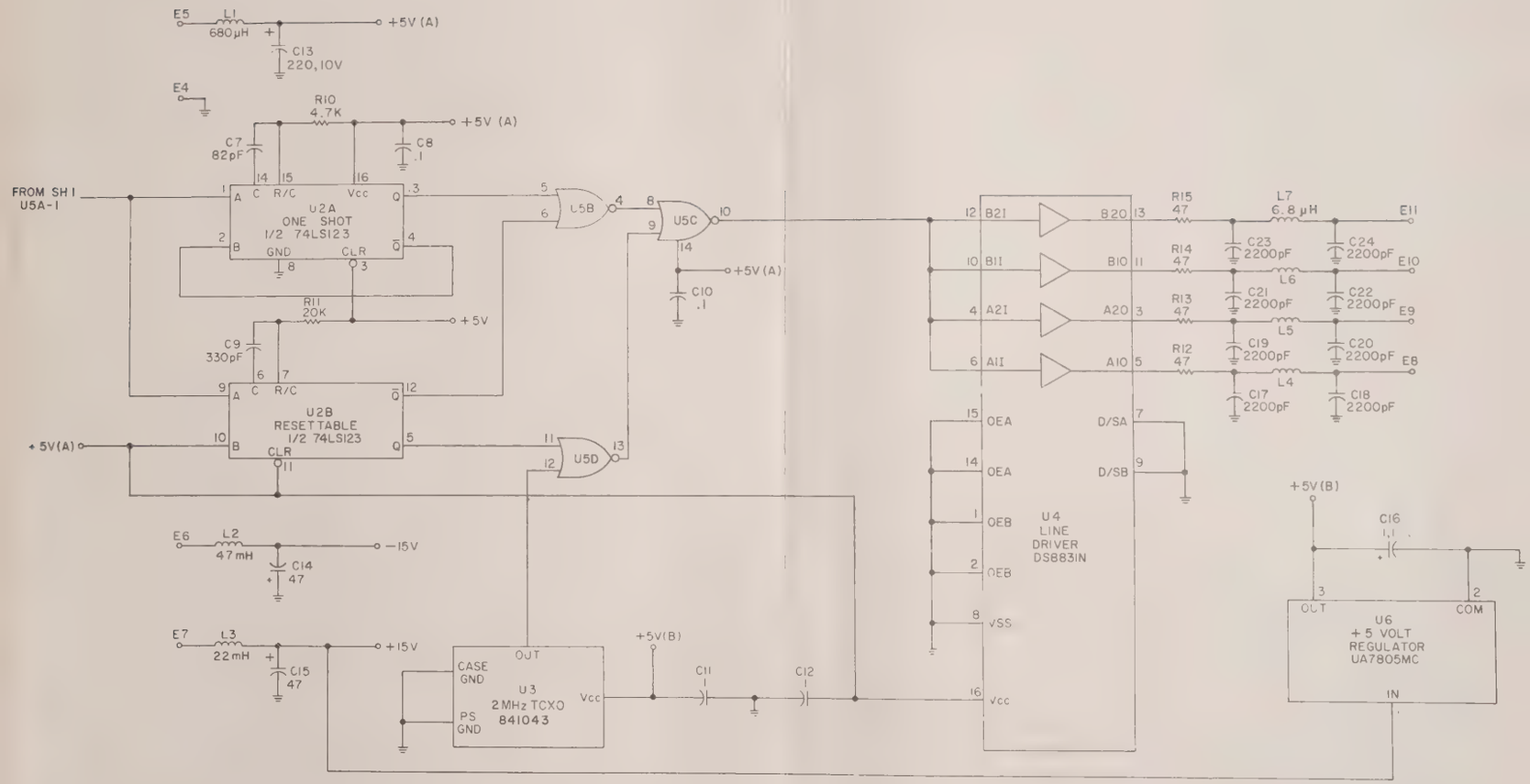


Figure 7-6. Part 380084 Reference Generator PC Assembly (A1A3A1), Schematic Diagram (Sheet 2 of 2)

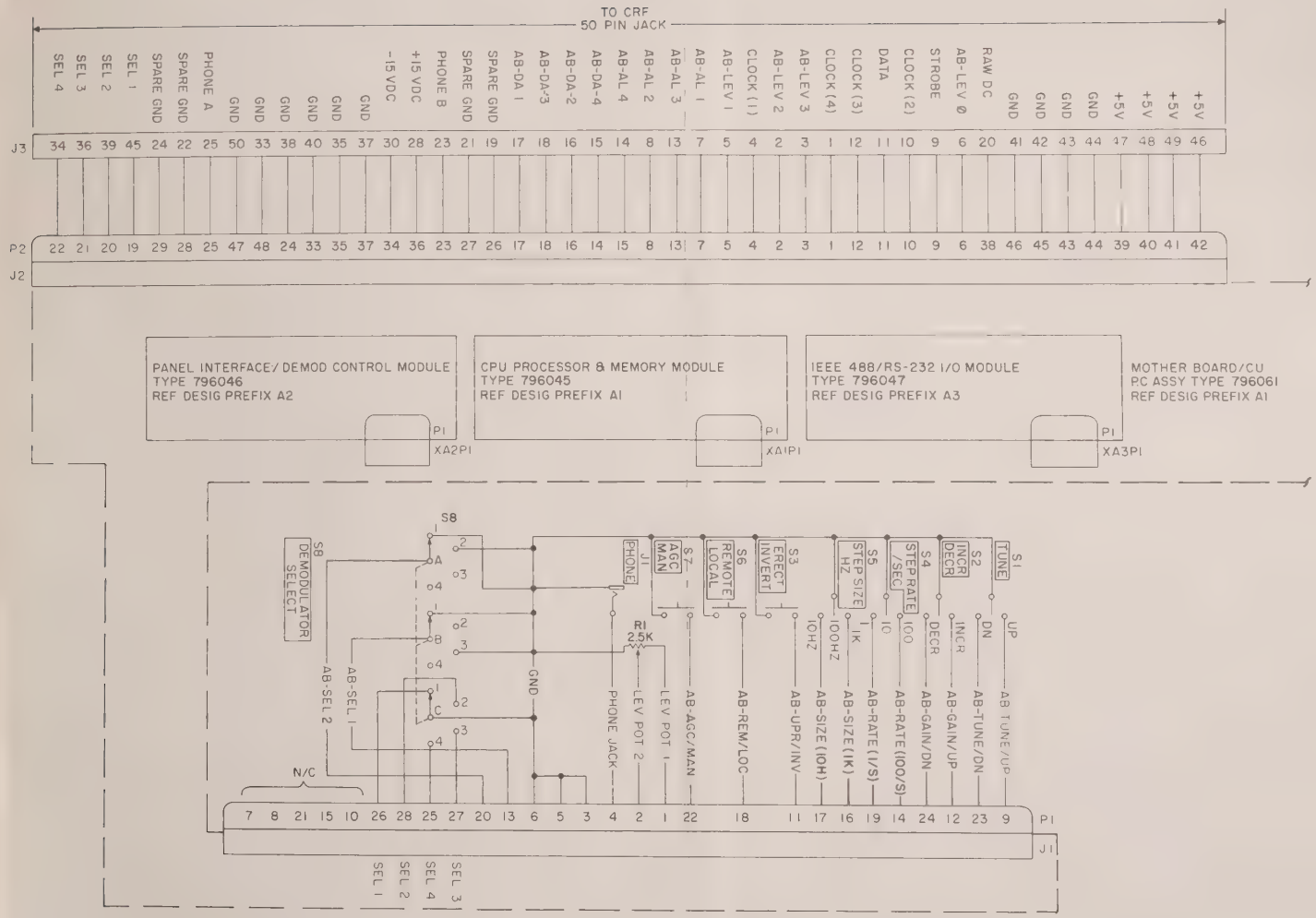


Figure 7-7. WJ-9525/CU Control Unit (A2), Schematic Diagram (Sheet 1 of 2)

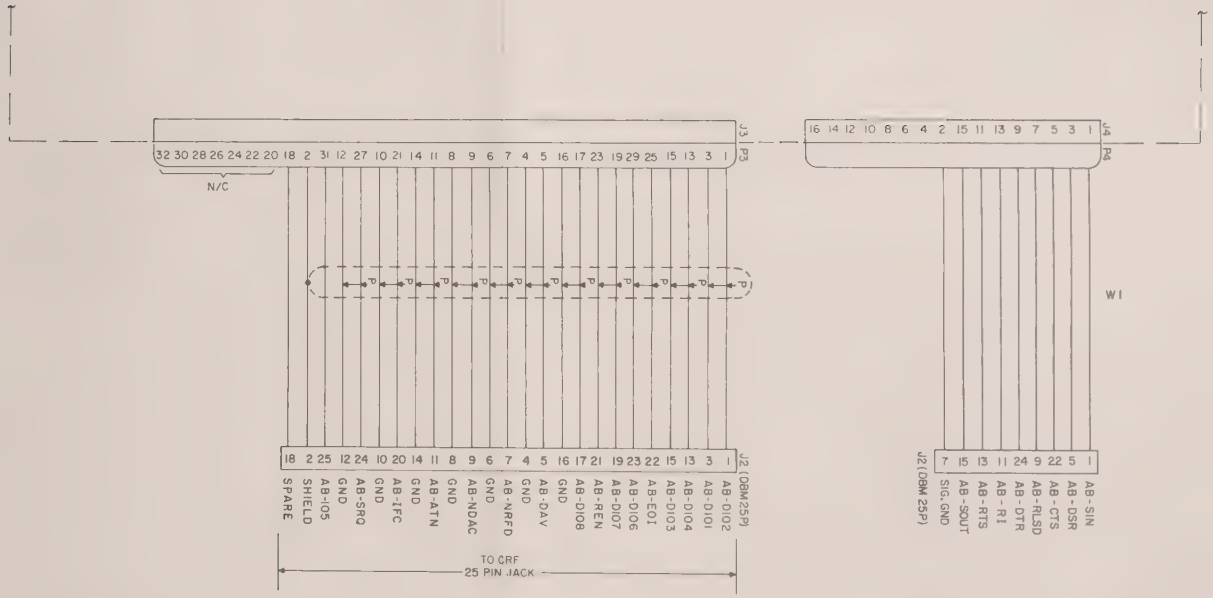


Figure 7-7. WJ-9525/CU Control Unit (A2), Schematic Diagram (Sheet 2 of 2)

NOTES
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, 5%, 1/8 W.
   b. CAPACITANCE IS IN µF.

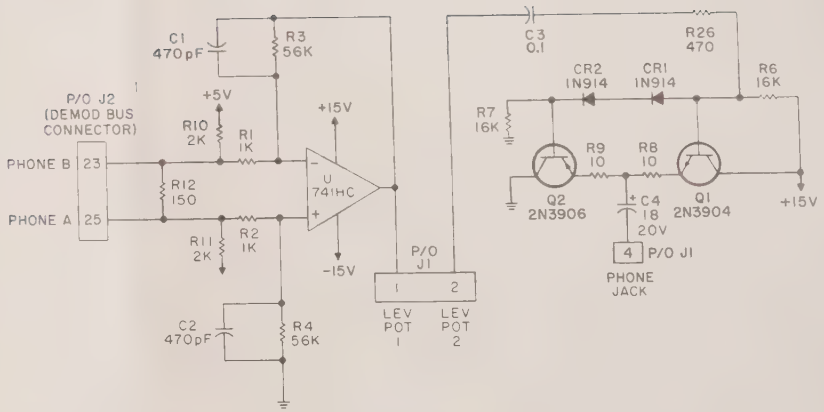


Figure 7-8. Type 796061 Motherboard (A2A1), Schematic Diagram (Sheet 1 of 3)

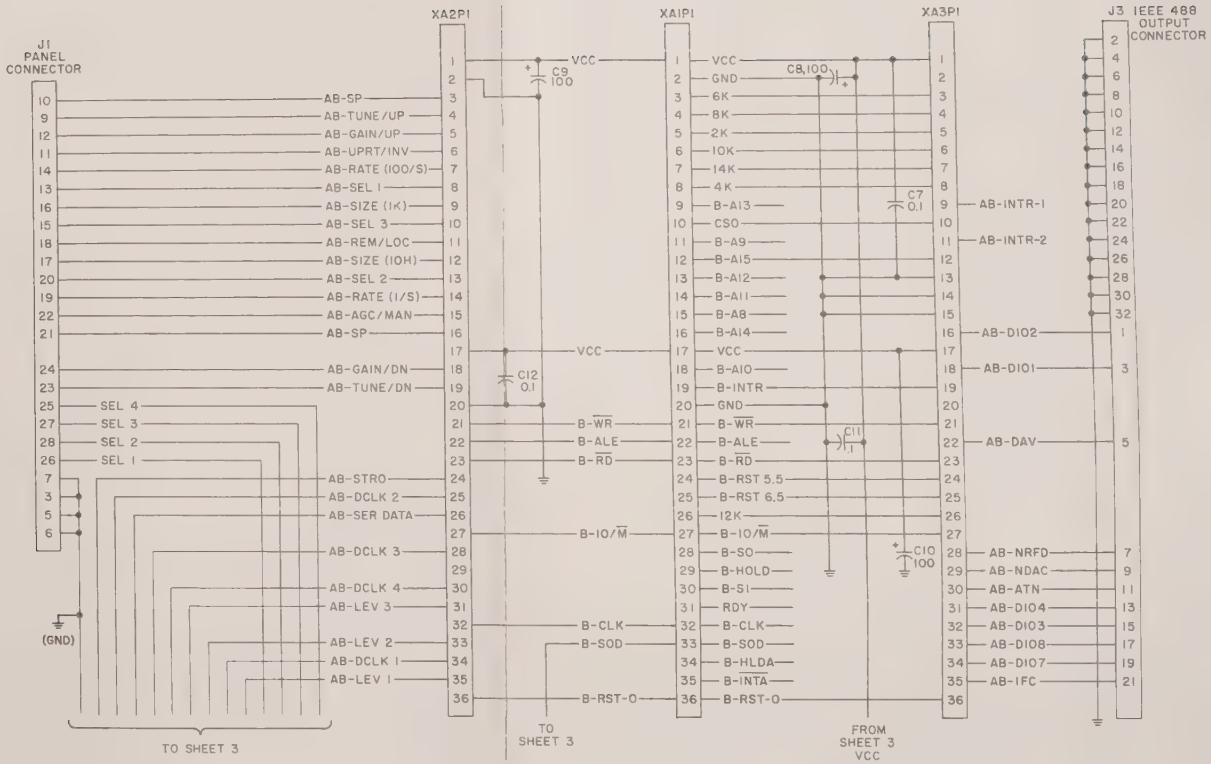


Figure 7-8. Type 796061 Motherboard (A2A1), Schematic Diagram (Sheet 2 of 3)

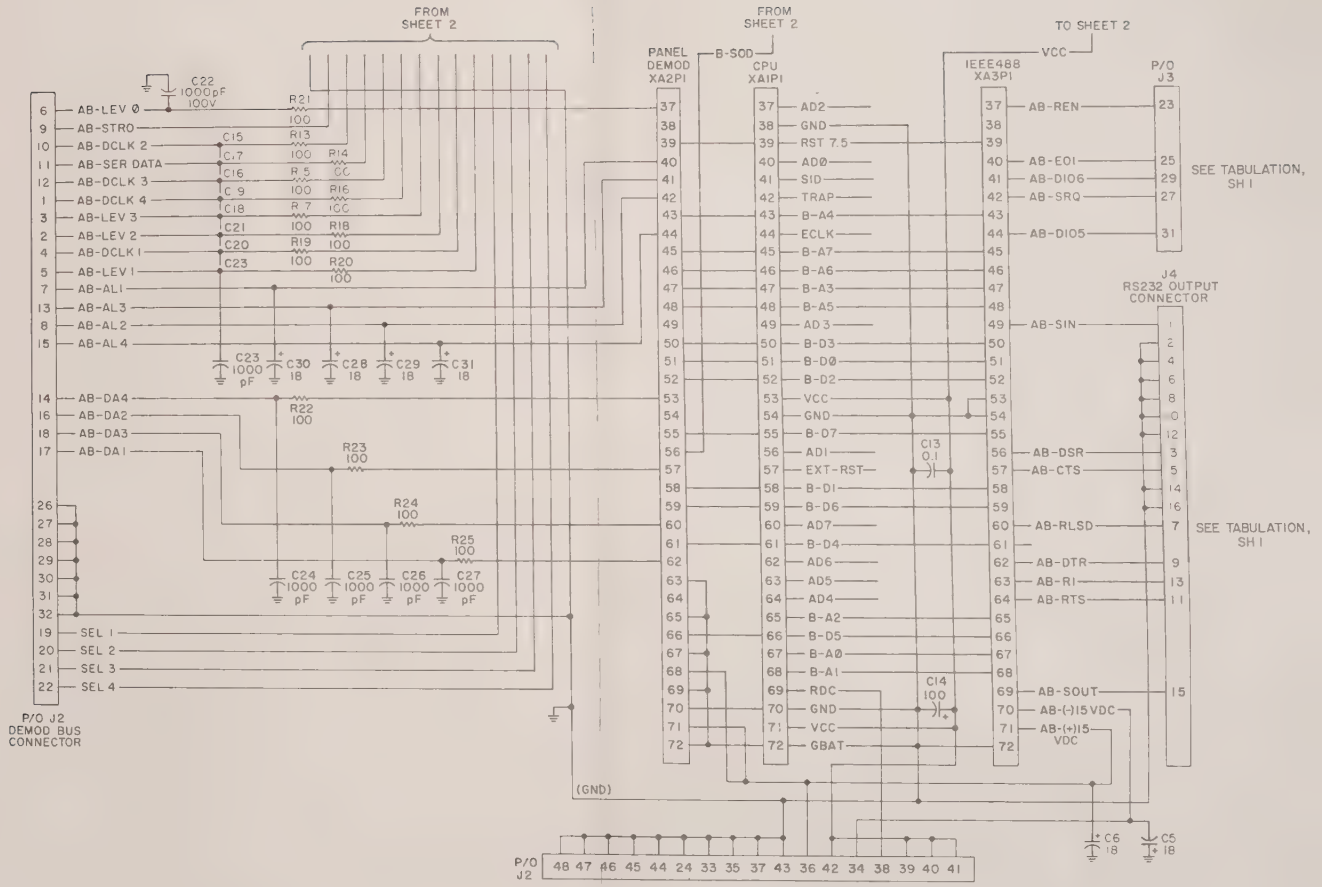
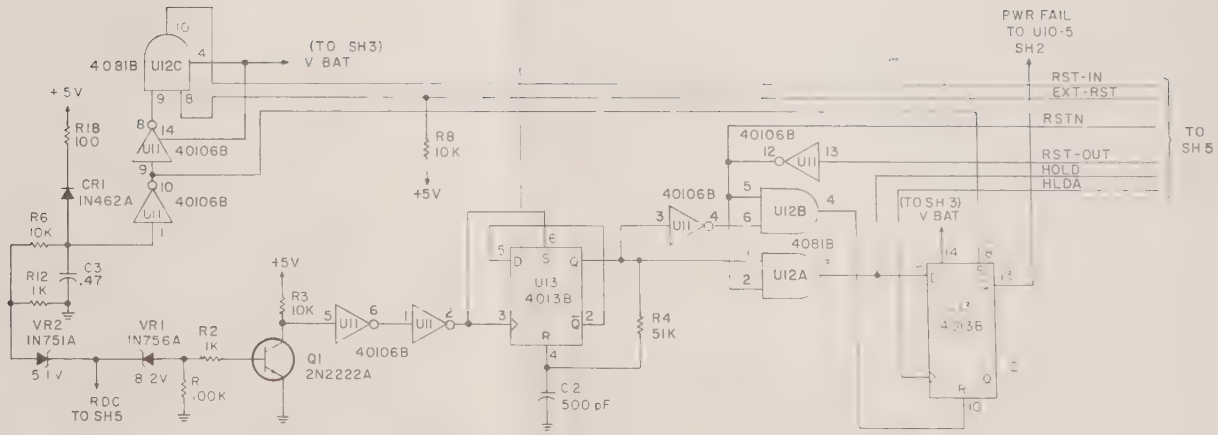


Figure 7-8. Type 796061 Motherboard (A2A1), Schematic Diagram (Sheet 3 of 3)



NOTES

1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W
   b) CAPICATANCE IS IN μF

Figure 7-9. Type 796045 CPU Processor and Memory (A2A1A1), Schematic Diagram (Sheet 1 of 5)

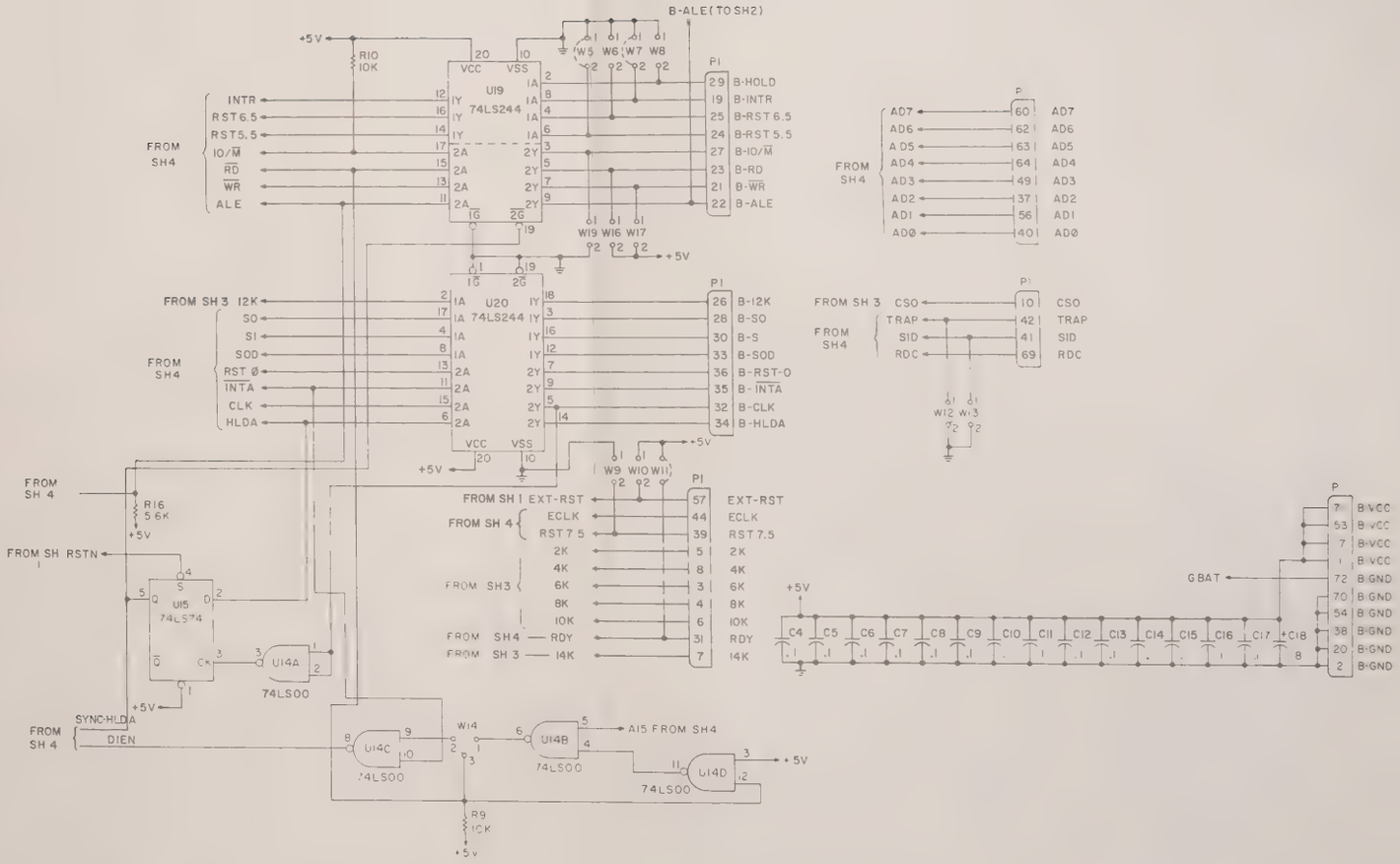


Figure 7-9. Type 796045 CPU Processor and Memory (A2A1A1), Schematic Diagram (Sheet 2 of 5)

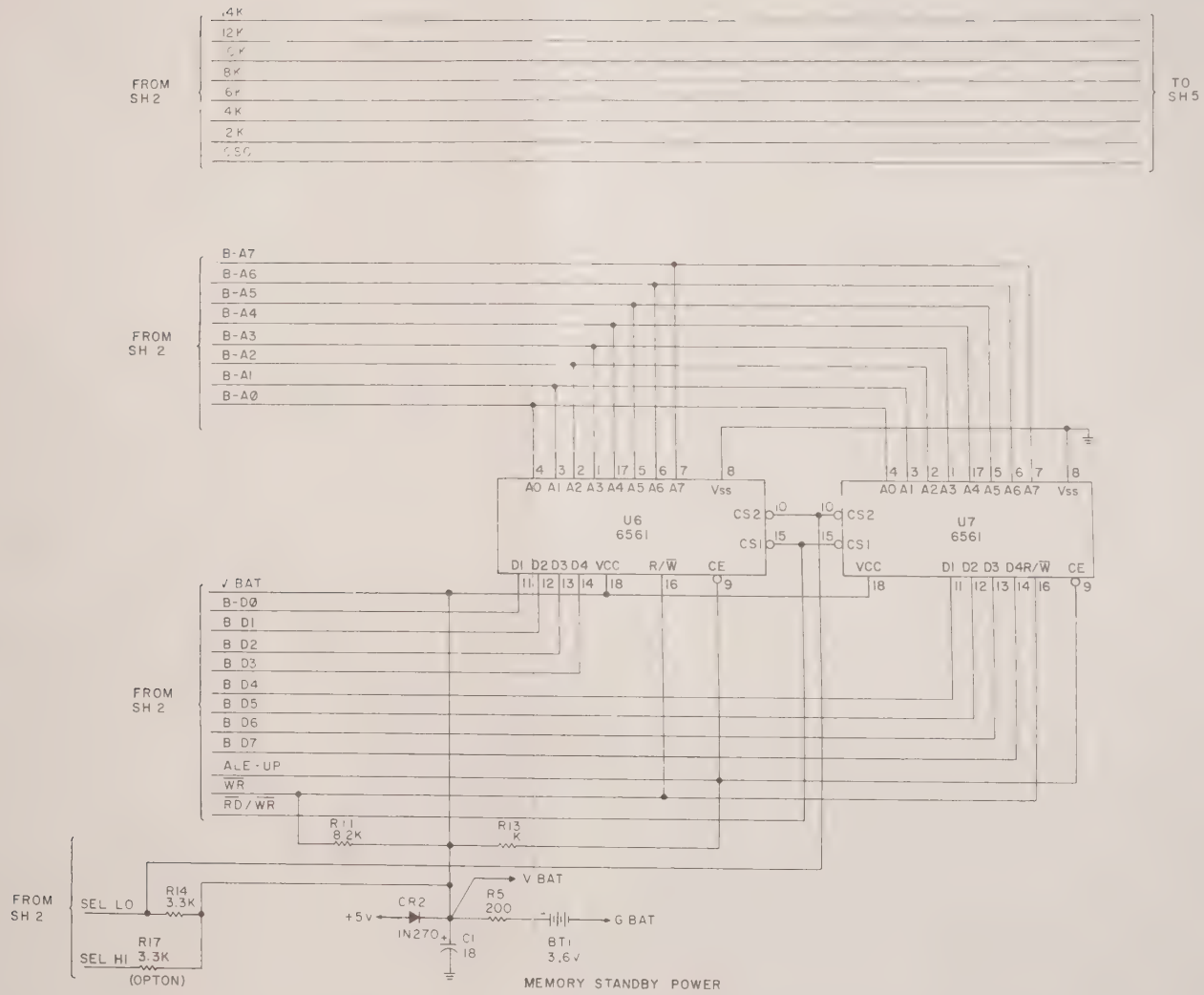


Figure 7-9. Type 796045 CPU Processor and Memory (A2A1A1), Schematic Diagram (Sheet 3 of 5)

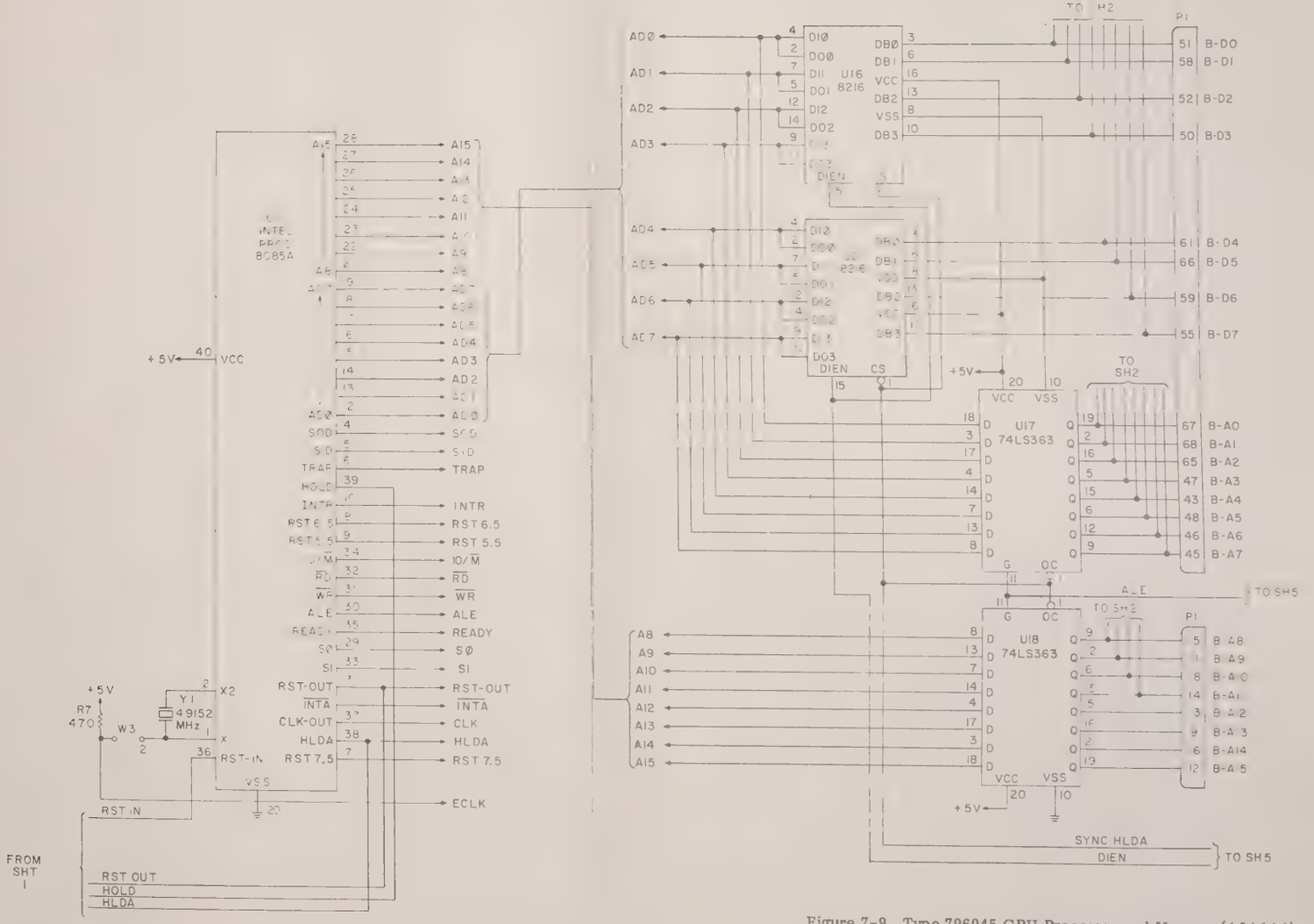


Figure 7-9. Type 796045 CPU Processor and Memory (A2A1A1), Schematic Diagram (Sheet 4 of 5)

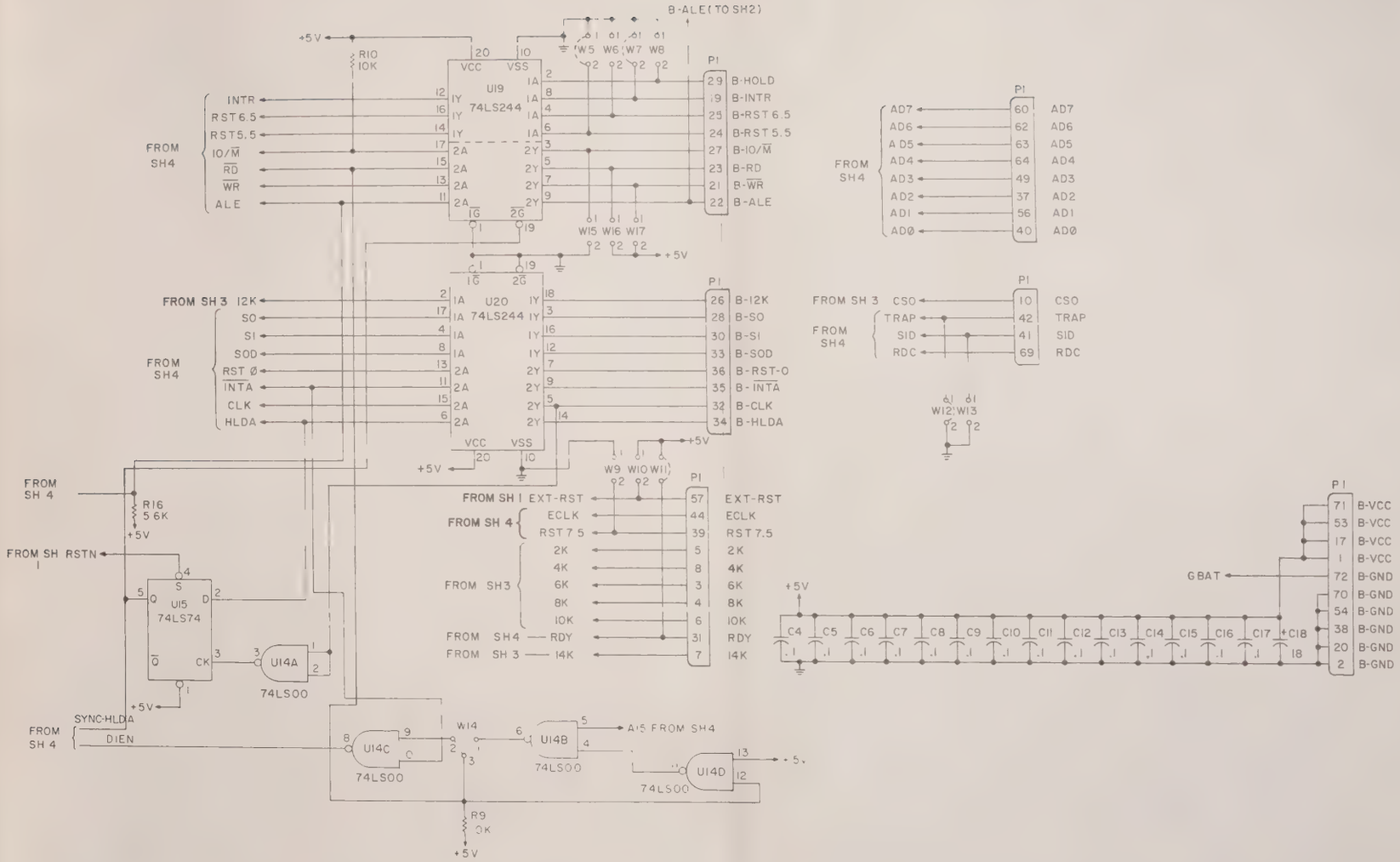


Figure 7-9. Type 796045 CPU Processor and Memory (A2A1A1), Schematic Diagram (Sheet 5 of 5)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN μF.
2. ONLY ONE SWITCH IS TO BE CLOSED AT ANY GIVEN TIME. THESE SWITCHES ARE OPTIONAL, AND NORMALLY NOT SUPPLIED WITH THE UNIT. THE APPROPRIATE CONNECTION IS MADE WITH JUMPER WIRES AS SHOWN.

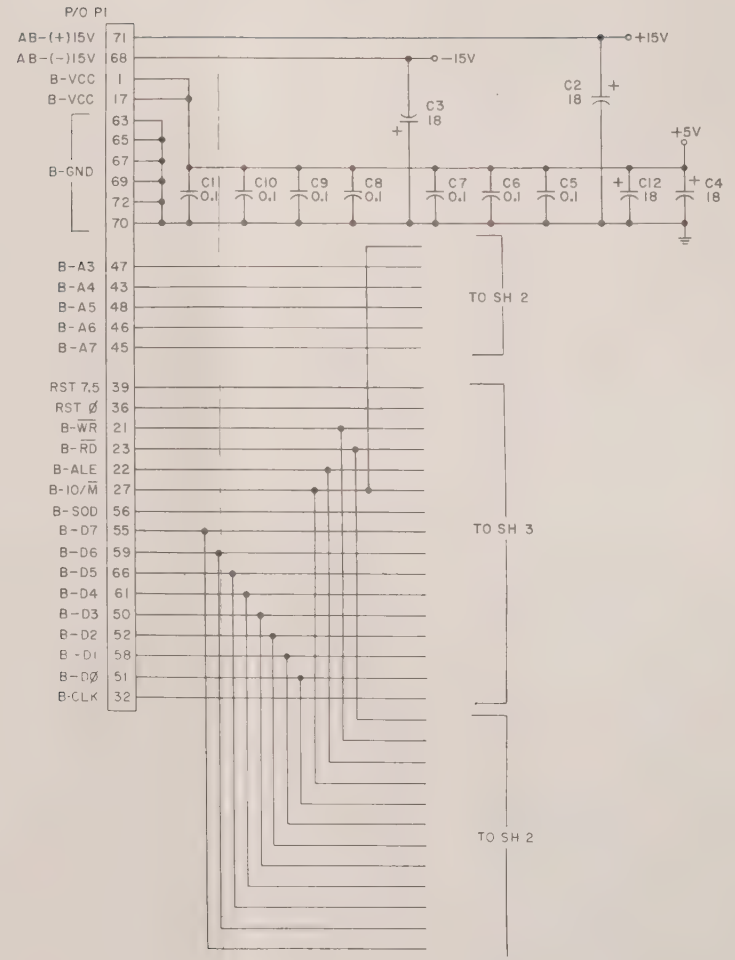


Figure 7-10. Type 796046 Panel Interface and Demodulator Control (A2A1A2), Schematic Diagram (Sheet 1 of 3)

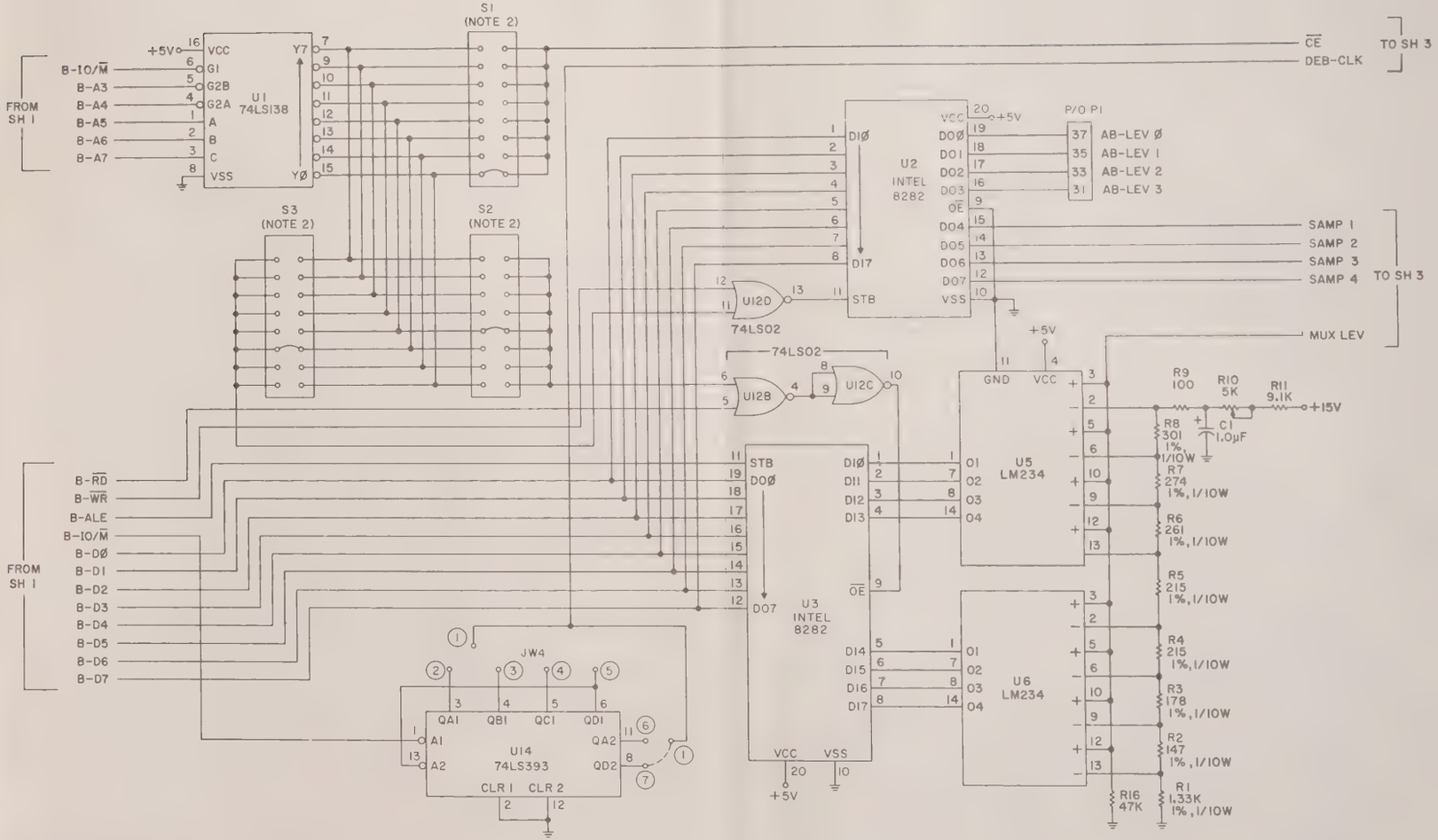


Figure 7-10. Type 796046 Panel Interface and Demodulator Control (A2A1A2), Schematic Diagram (Sheet 2 of 3)

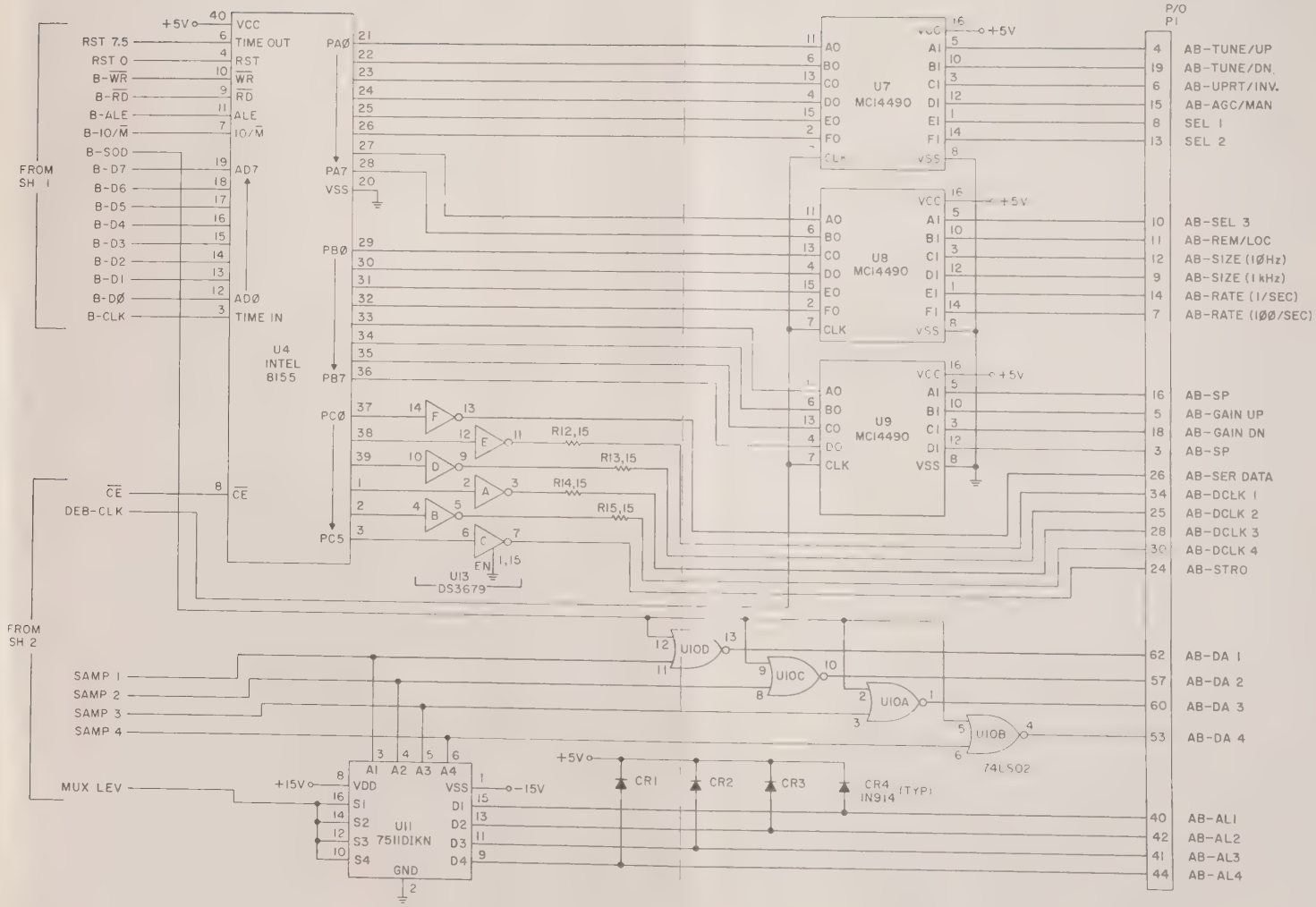
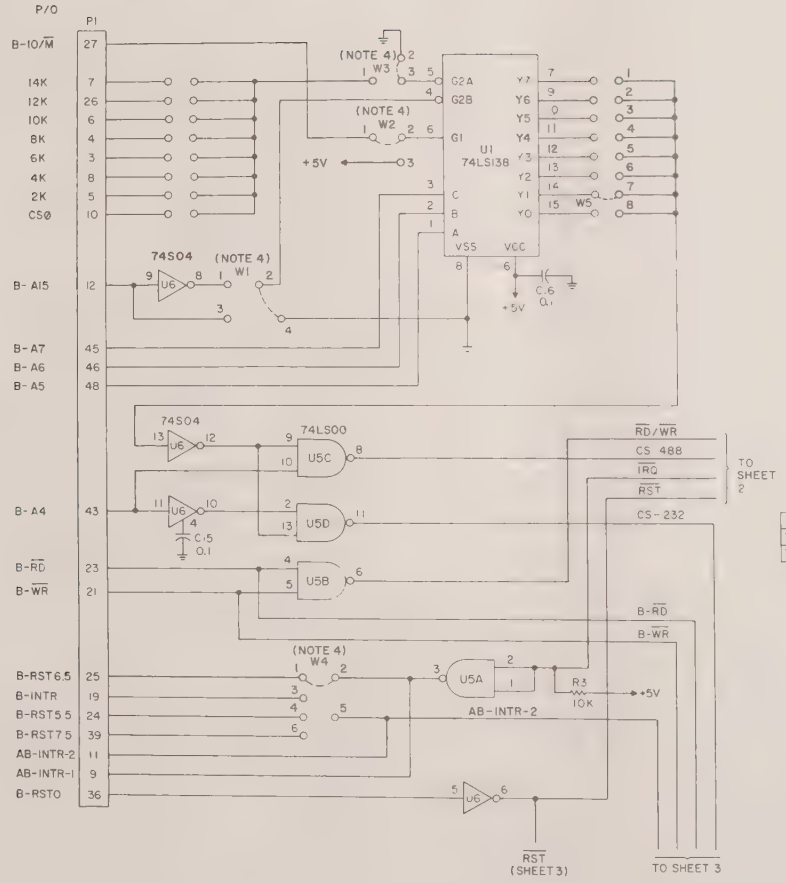


Figure 7-10. Type 796046 Panel Interface and Demodulator Control (A2A1A2), Schematic Diagram (Sheet 3 of 3)



NOTES:
1. ALL DASHED AREA IS OPTIONAL ON SHEET
2. UNUSED INPUTS ON U4 AND U14 ARE CONNECTED TO GROUND
3. UNLESS OTHERWISE SPECIFIED
   a. RESISTANCE IS IN OHMS 5%, 1/4 W.
   b. CAPACITANCE IS IN μF.
4. DIFFERENCE BETWEEN TYPES IS SHOWN IN TABLES A & B.

TABLE A

	W1	W2	W3	W4	NOTE
796047-1	2-4	1-2	2-3	1-2	FOR 488, INT 6.5 (AS SHOWN)
796047-2	2-4	1-2	2-3	4-5	FOR RS-232, INT 5.5

TABLE B

	REF. DESIG. NOT USED:
796047-1	C1,C2,C3,C4,C5,C6,C7,C10,C11,C12 R1,R2 S1,S2 U4,U8,U13 Y1
796047-2	C13,C14 S1,S2,S3 U2,U3,U7,U9,U10,U11,U12

Figure 7-11. Type 796047-1 IEEE 488/RS-232 Input/Output (A2A1A3), Schematic Diagram (Sheet 1 of 3)

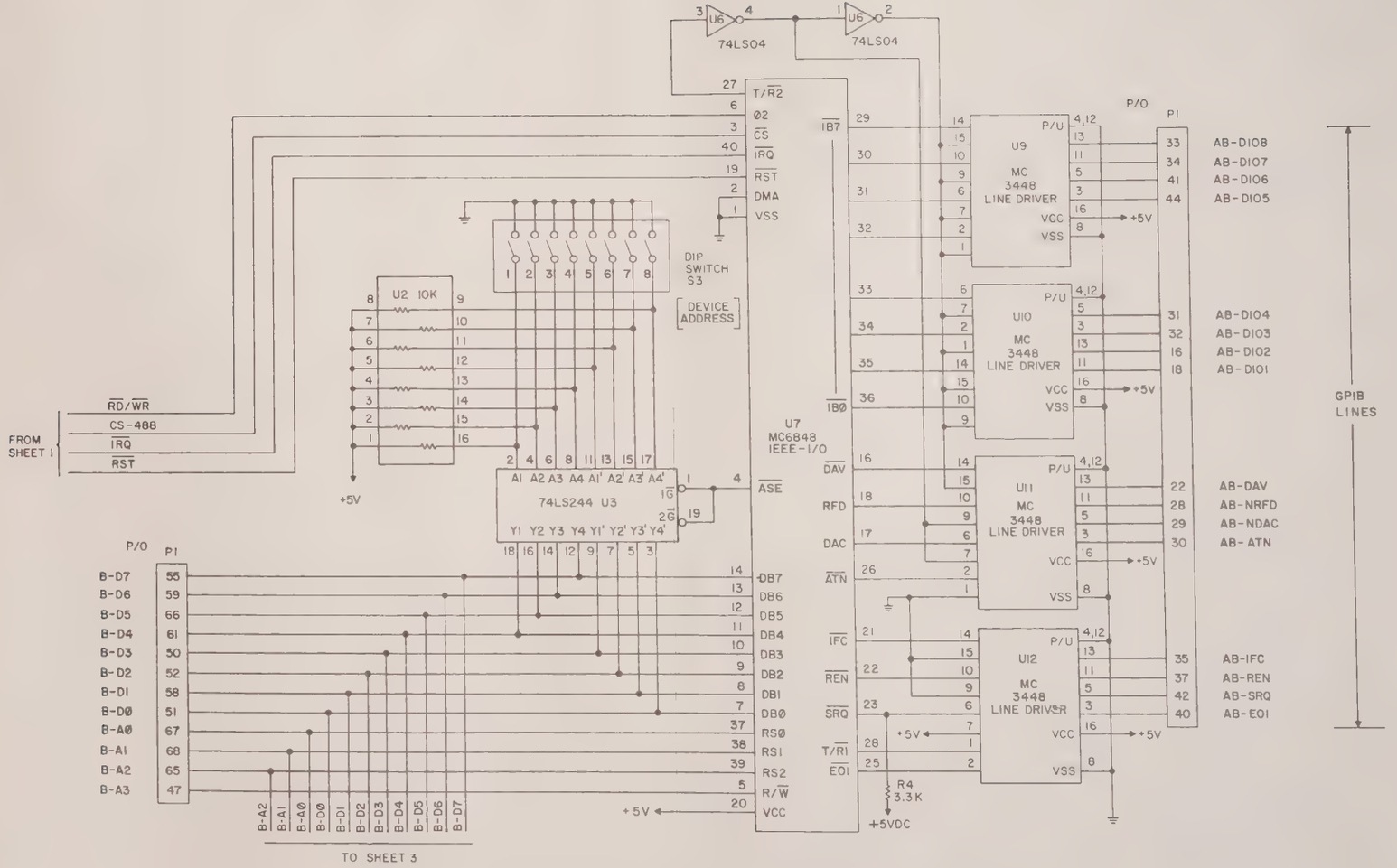


Figure 7-11. Type 796047-1 IEEE 488/RS-232 Input/Output (A2A1A3), Schematic Diagram (Sheet 2 of 3)

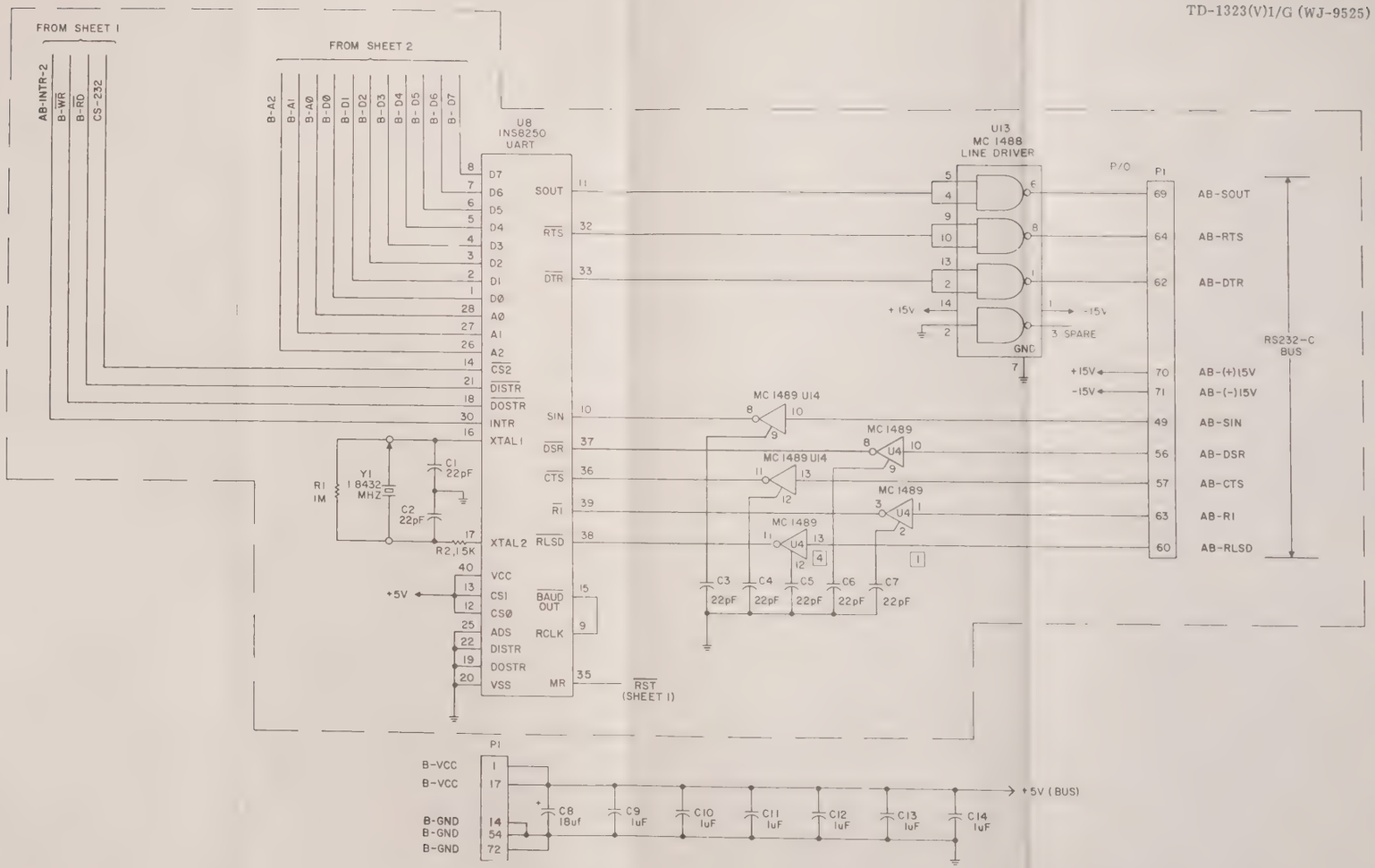
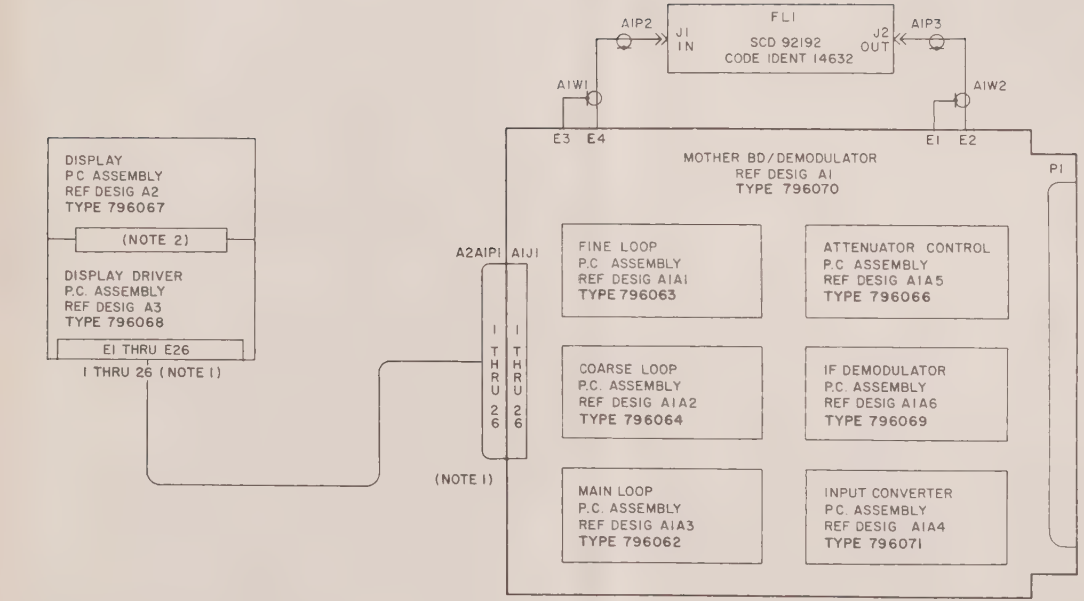


Figure 7-11. Type 796047-1 IEEE 488/RS-232 Input/Output (A2A1A3), Schematic Diagram (Sheet 3 of 3)



NOTES:

1. A2A1E1 THRU A2A1E26, A2A1P1 AND A1J1 ARE CONNECTED PIN FOR PIN.
2. SEE SCHEM 480085 FOR DETAILED INTERCONNECTION BETWEEN DISPLAY & DISPLAY DRIVER

Figure 7-12. WJ-9525/DU Demodulator Unit (A3, A4, A5, A6), Schematic Diagram

NOTES:
1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE IS IN OHMS ±5%
   b) CAPICATANCE IS IN μF
2. ON A2 COURCE LOOP GROUND THE FOLLOWING PINS, P1-8 THRU P1-16, P2-9
3. ON A3 MAIN LOOP, GROUND THE FOLLOWING PINS P1-4, P1-5, P1-8 THRU P1-13, P1-15 THRU P1-17, P2-6 THRU P2-12, P2-14.
4. ON A1 FINE LOOP, GROUND THE FOLLOWING PINS P2-2 THRU P2-14

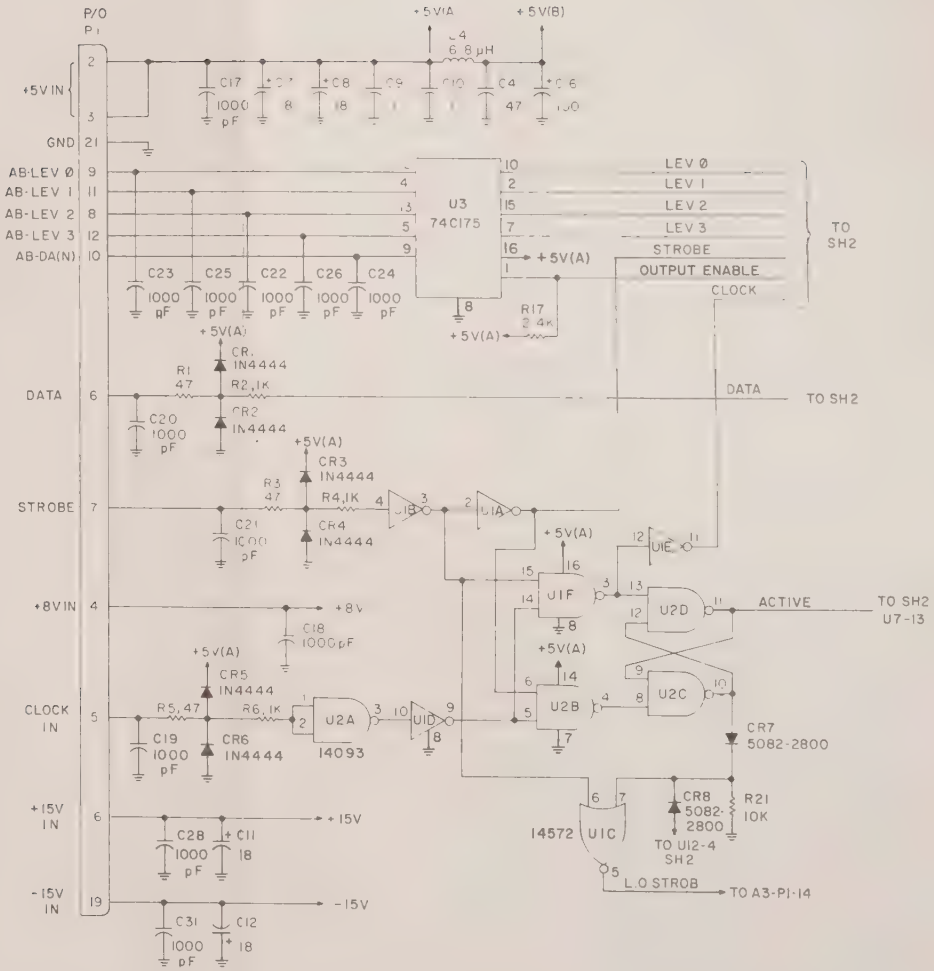


Figure 7-13. Type 796070 Motherboard (A3A1), Schematic Diagram (Sheet 1 of 3)

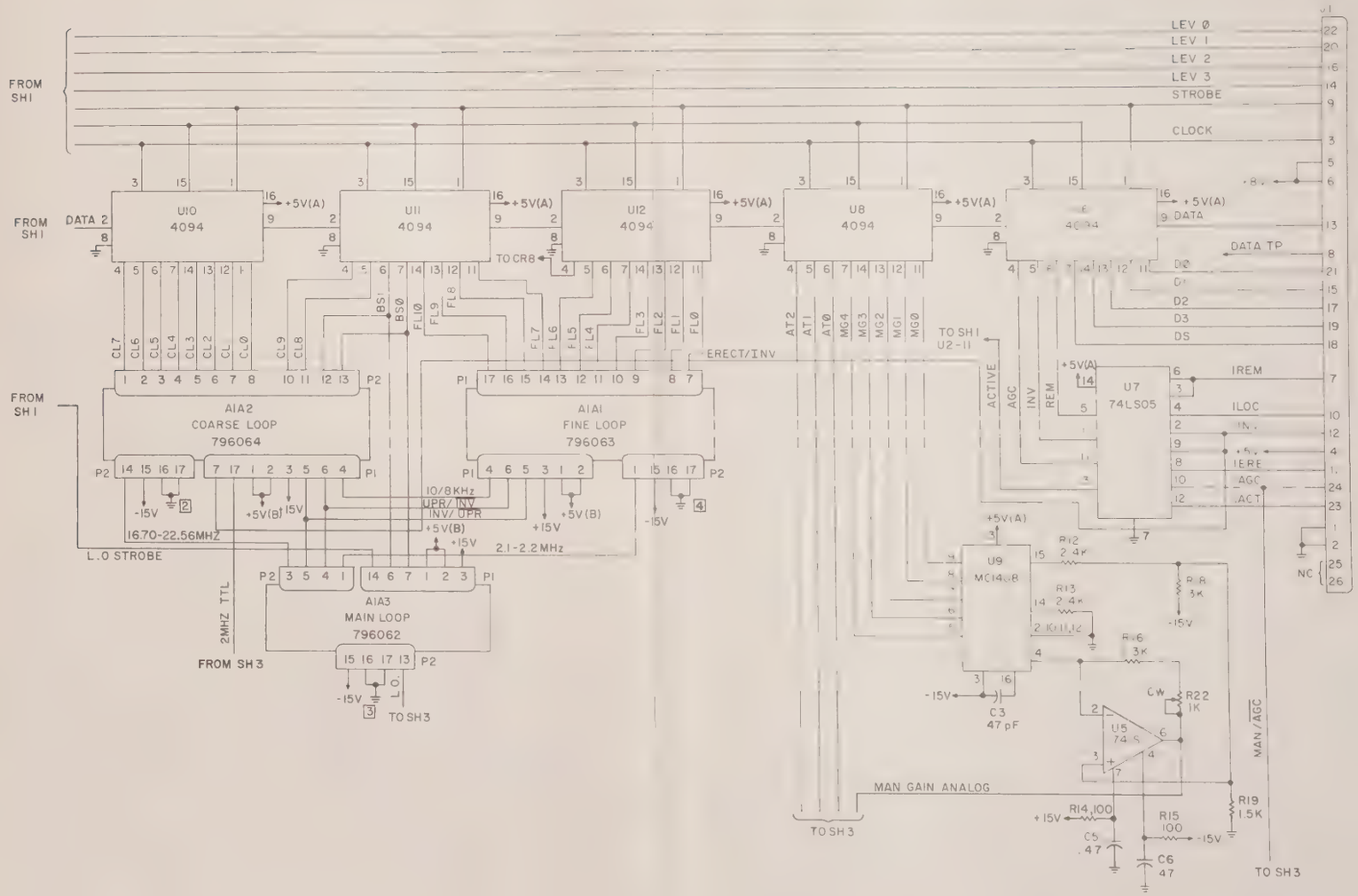
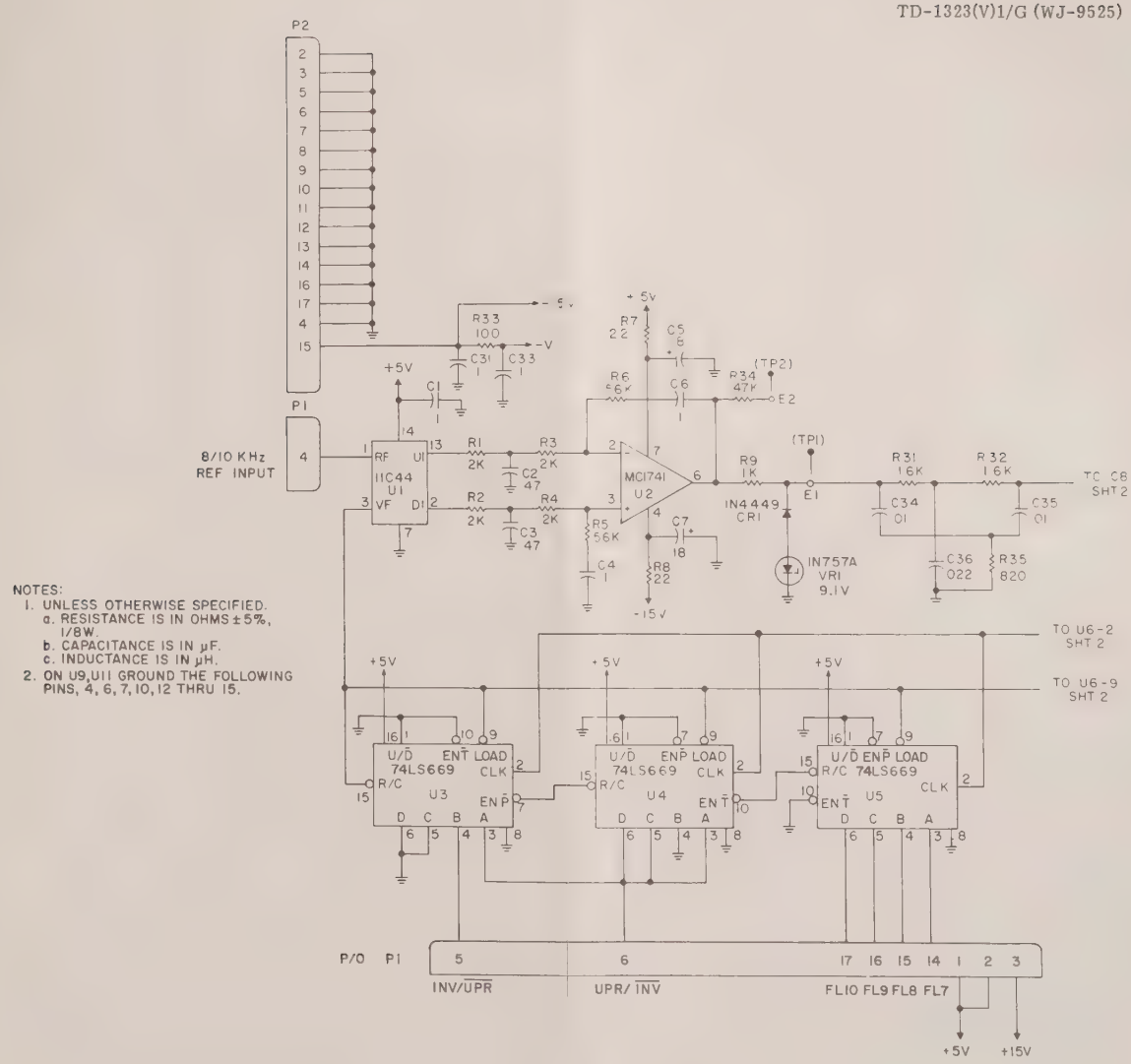


Figure 7-13. Type 796070 Motherboard (A3A1), Schematic Diagram (Sheet 2 of 3)



NOTES:
1. UNLESS OTHERWISE SPECIFIED.
   a. RESISTANCE IS IN OHMS ±5%, 1/8W.
   b. CAPACITANCE IS IN μF.
   c. INDUCTANCE IS IN μH.
2. ON U9,U11 GROUND THE FOLLOWING PINS, 4, 6, 7, 10, 12 THRU 15.

Figure 7-14. Type 796063 Fine Loop (A3A1A1), Schematic Diagram (Sheet 1 of 2)

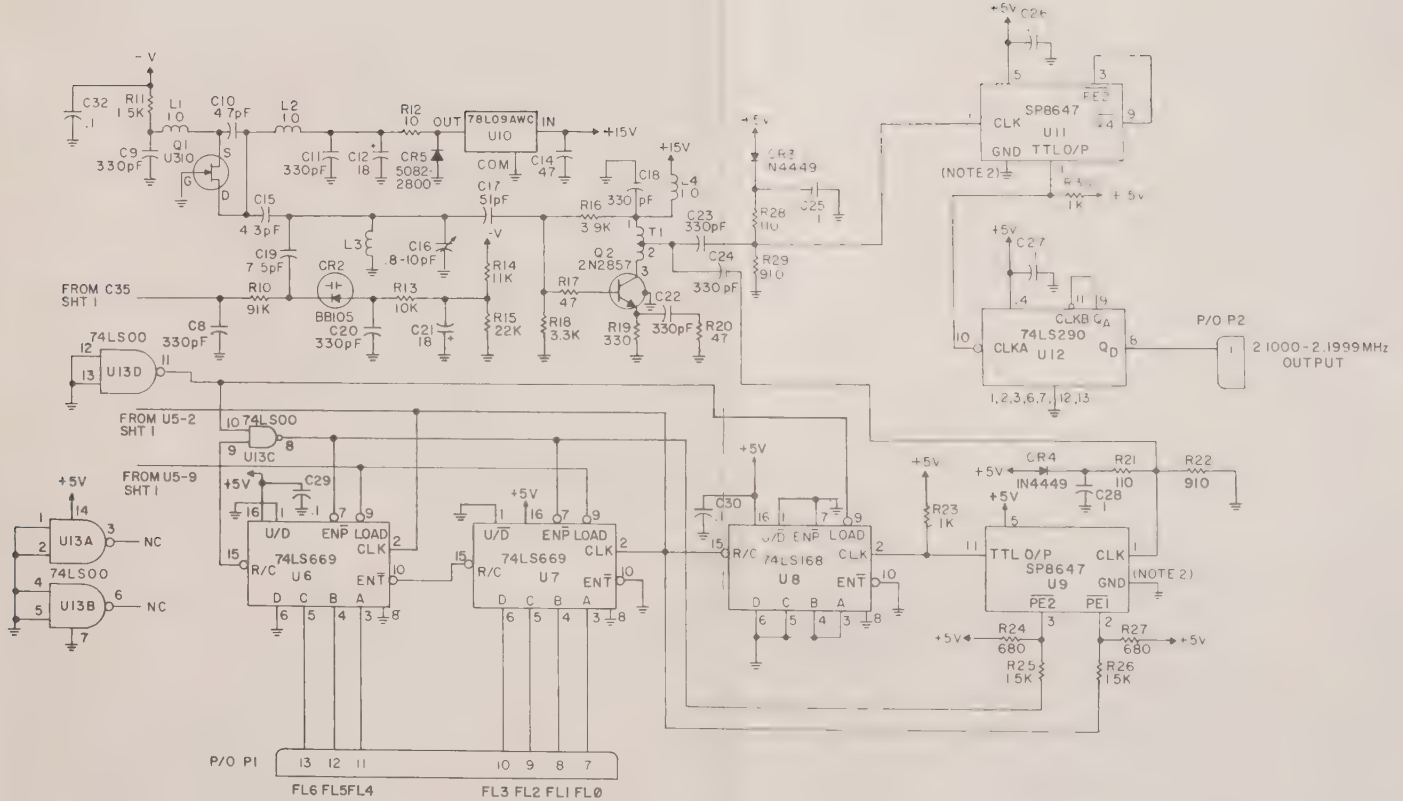


Figure 7-14. Type 796063 Fine Loop (A3A1A1), Schematic Diagram (Sheet 2 of 2)

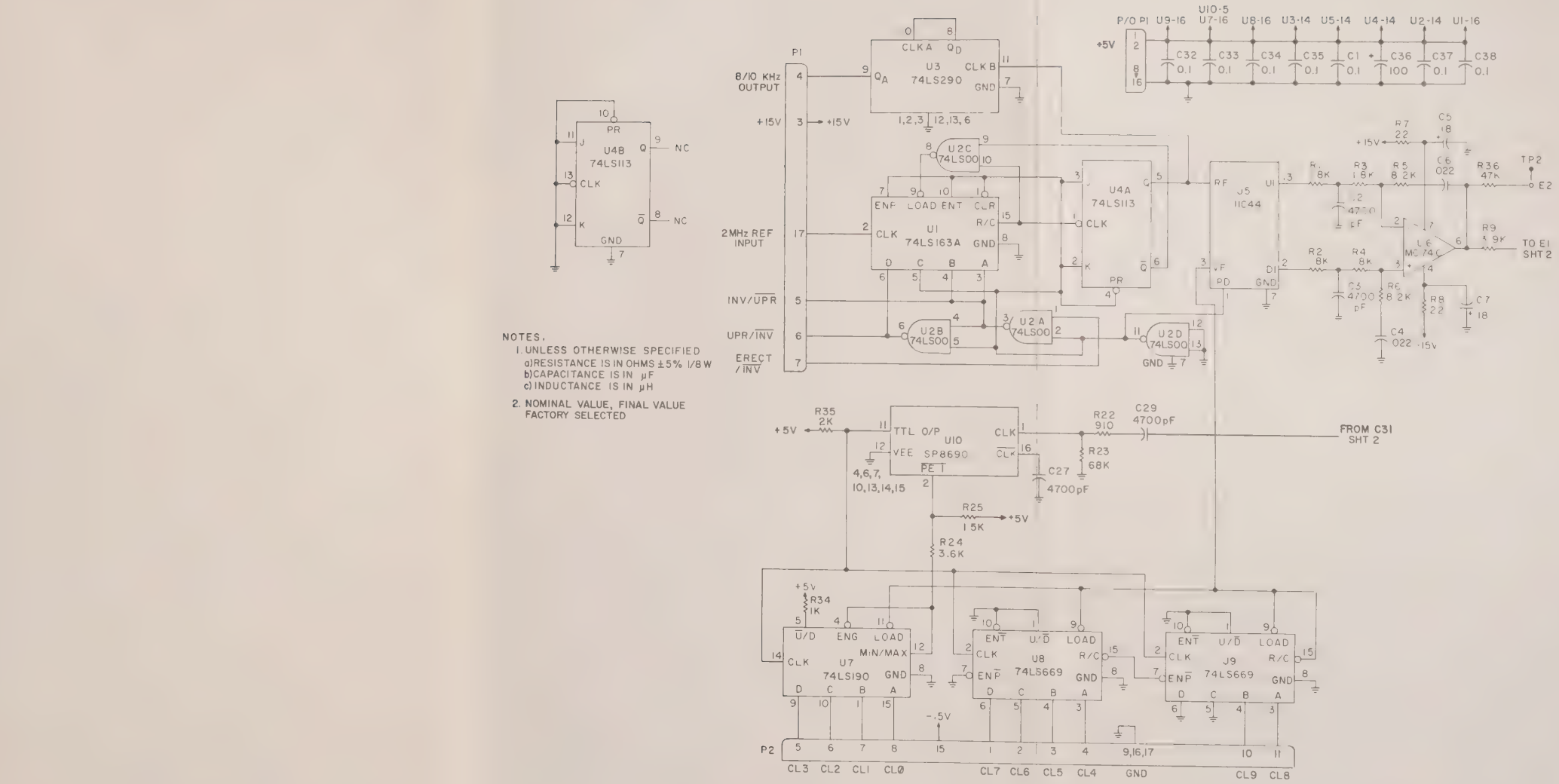


Figure 7-15. Type 796064 Coarse Loop (A3A1A2), Schematic Diagram (Sheet 1 of 2)

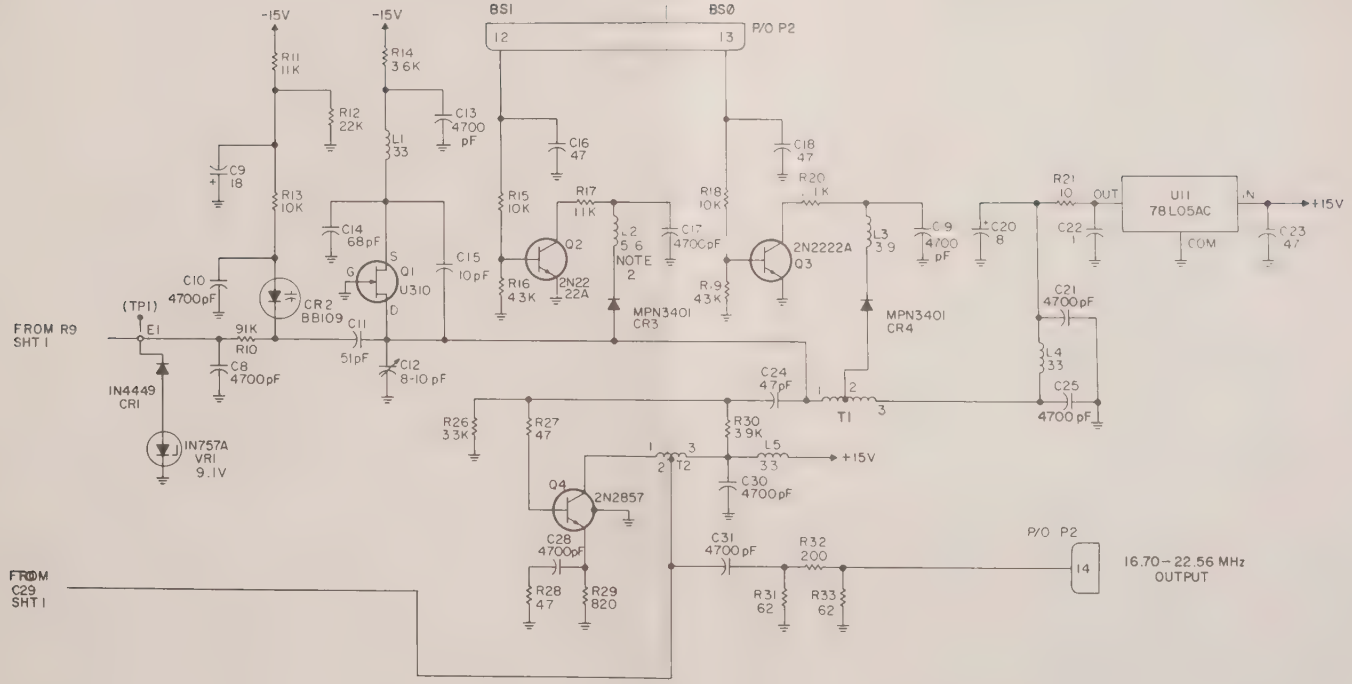


Figure 7-15. Type 796064 Coarse Loop (A3A1A2), Schematic Diagram (Sheet 2 of 2)

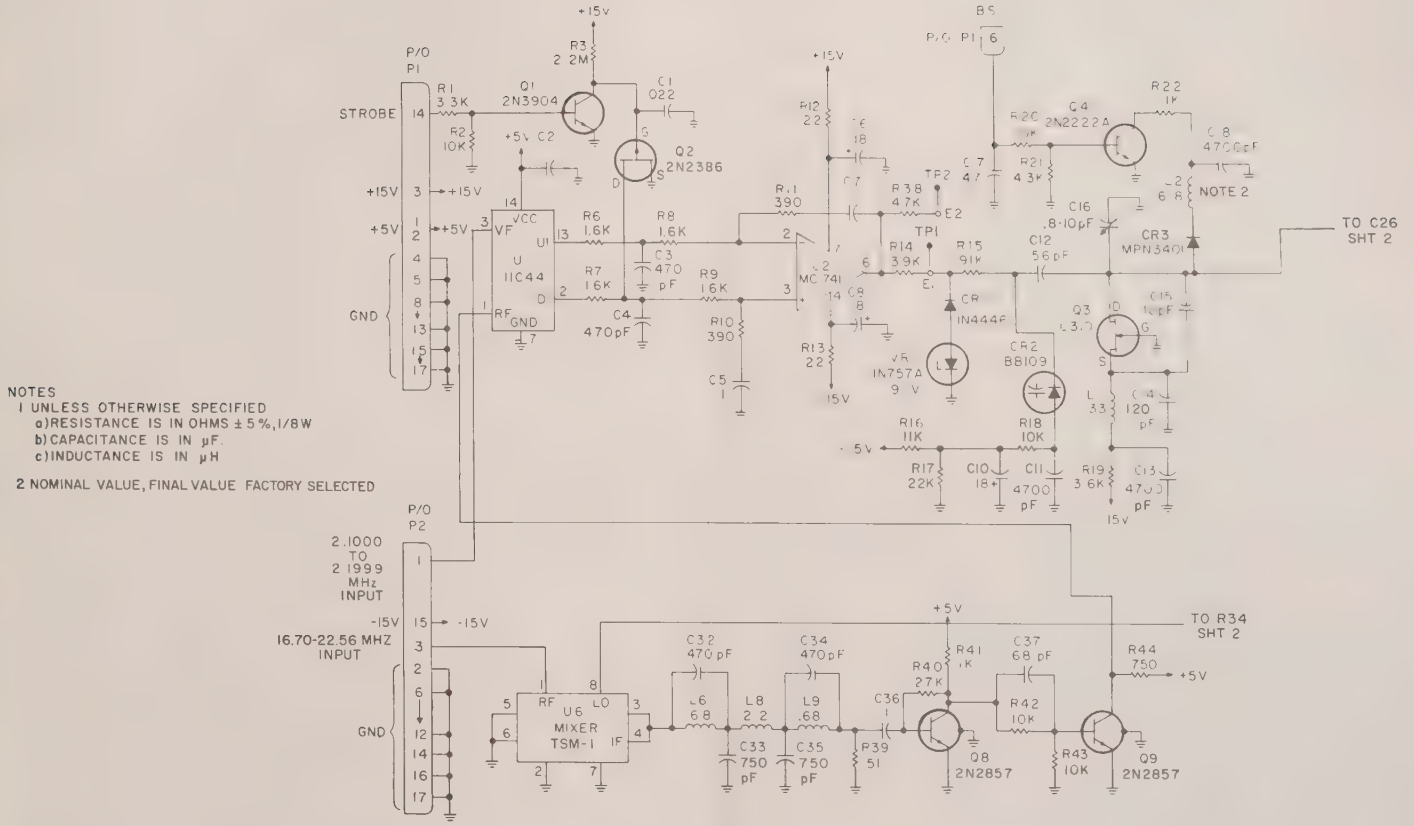


Figure 7-16. Type 796062 Main Loop (A3A1A3), Schematic Diagram (Sheet 1 of 2)

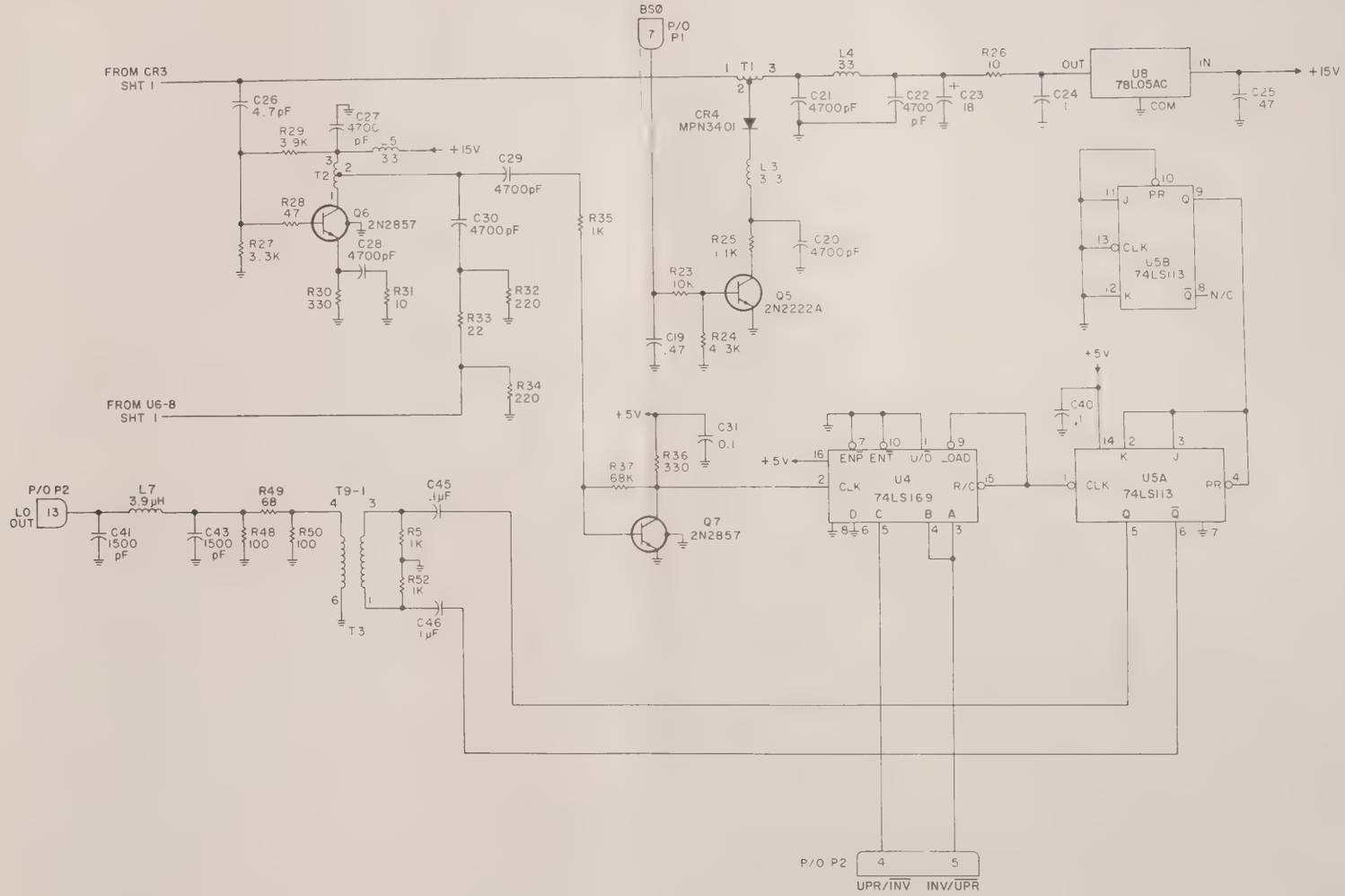


Figure 7-16. Type 796062 Main Loop (A3A1A3), Schematic Diagram (Sheet 2 of 2)

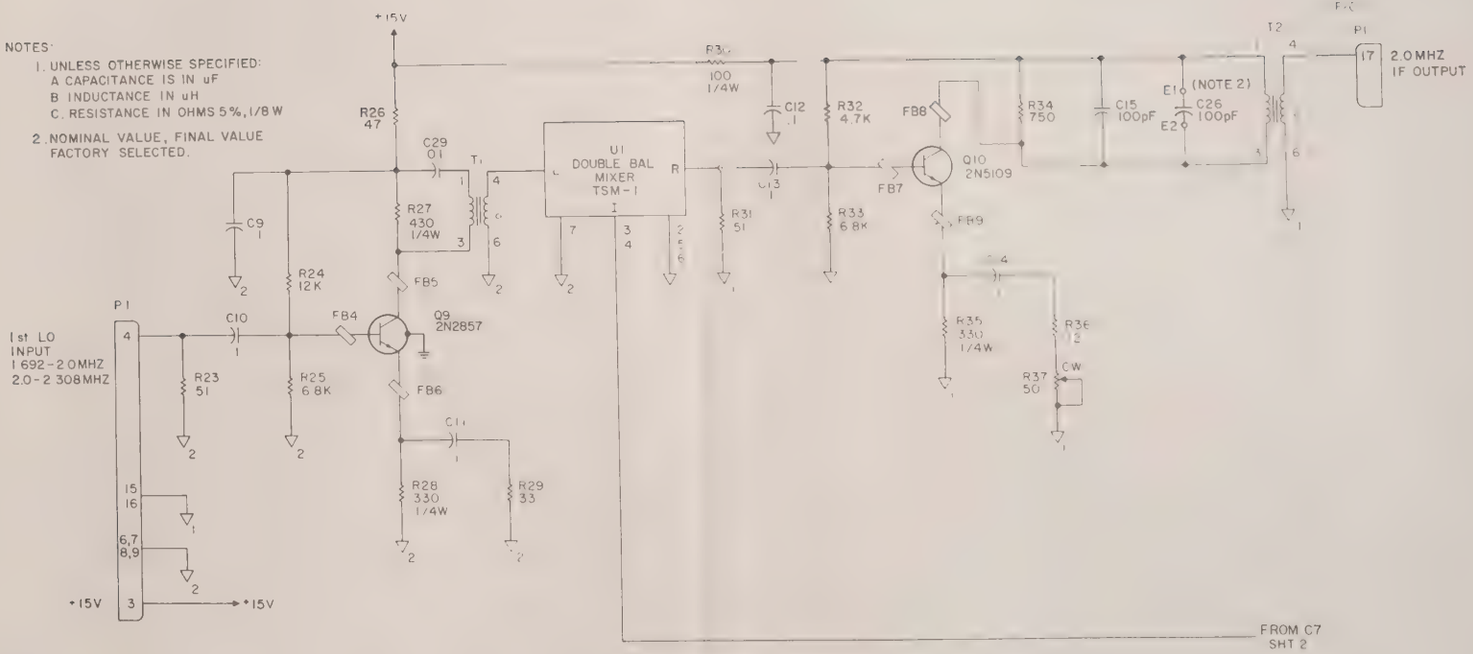


Figure 7-17. Type 796071 Input Converter (A3A1A4), Schematic Diagram (Sheet 1 of 3)

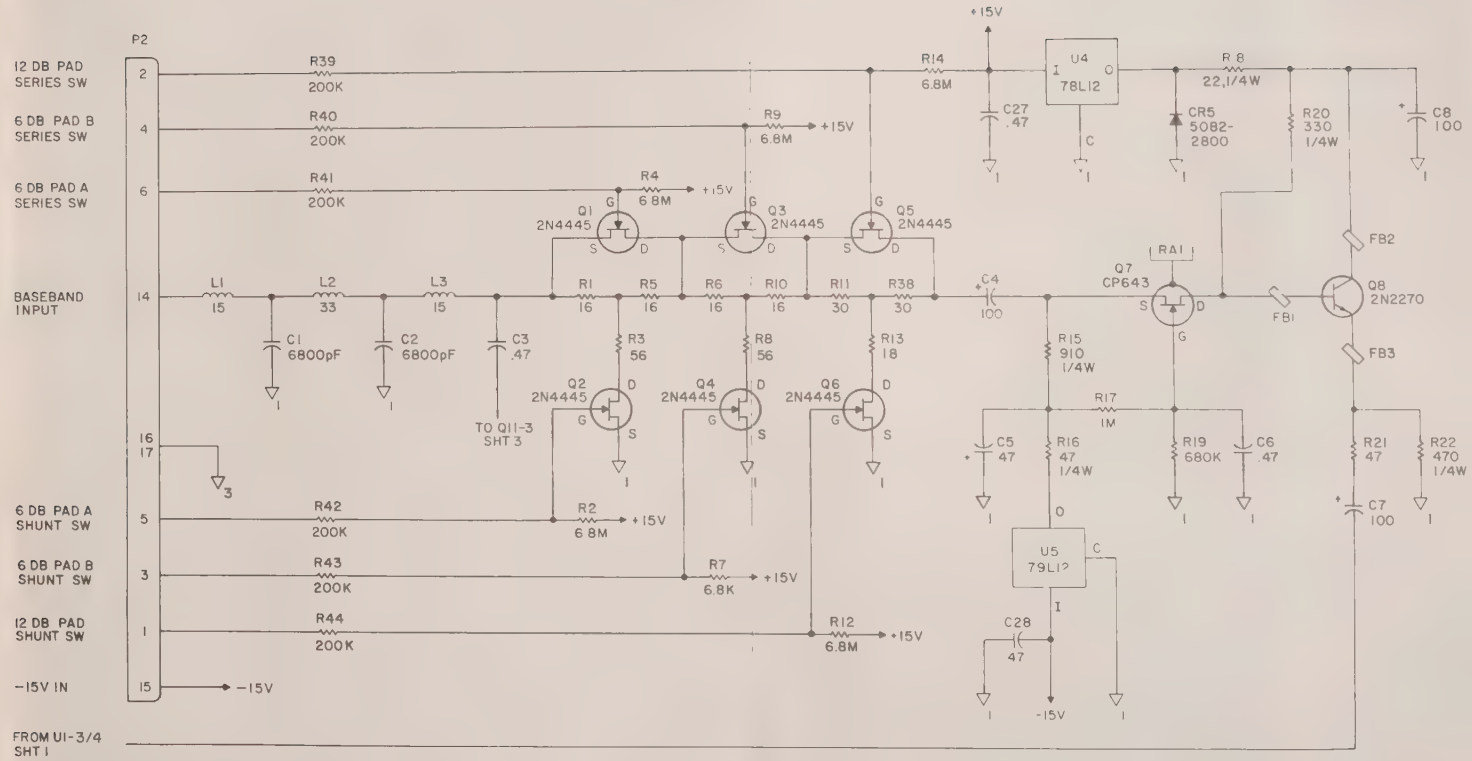


Figure 7-17. Type 796071 Input Converter (A3A1A4), Schematic Diagram (Sheet 2 of 3)

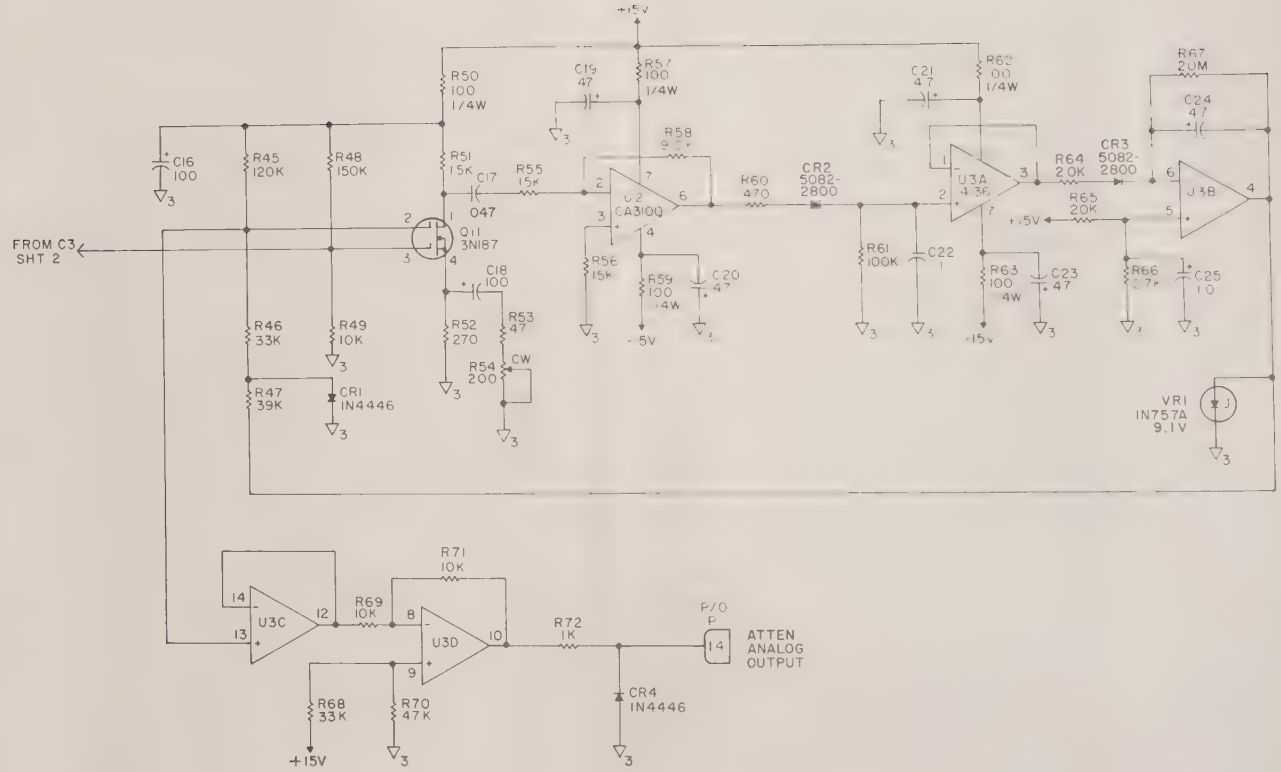


Figure 7-17. Type 796071 Input Converter (A3A1A4), Schematic Diagram (Sheet 3 of 3)

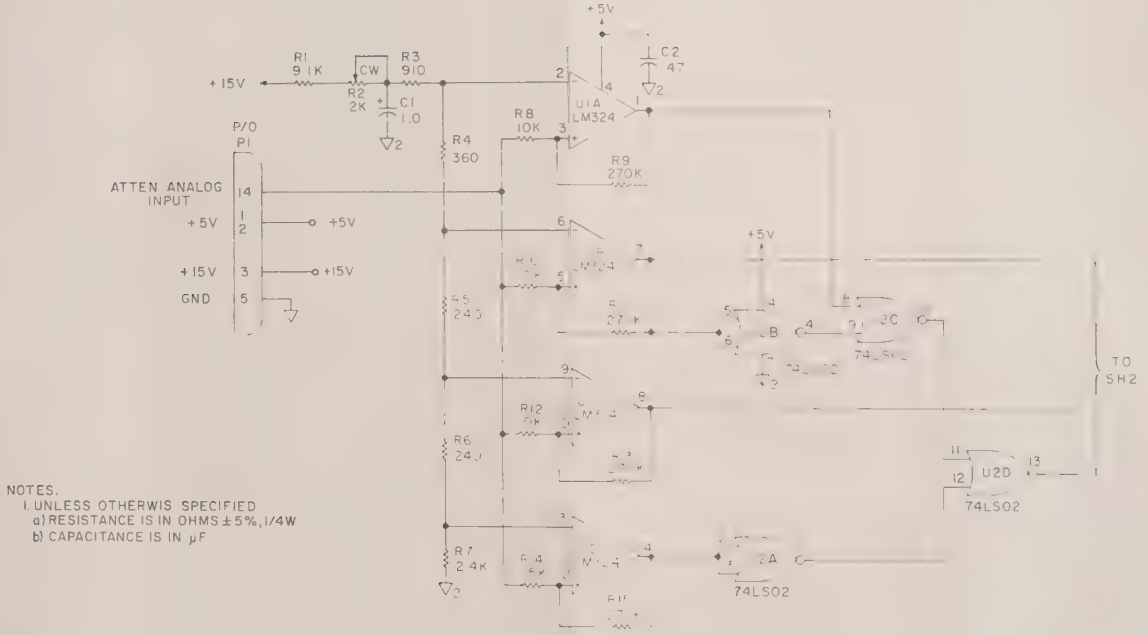


Figure 7-18. Type 796066 Attenuator Control (A3A1A5), Schematic Diagram (Sheet 1 of 2)

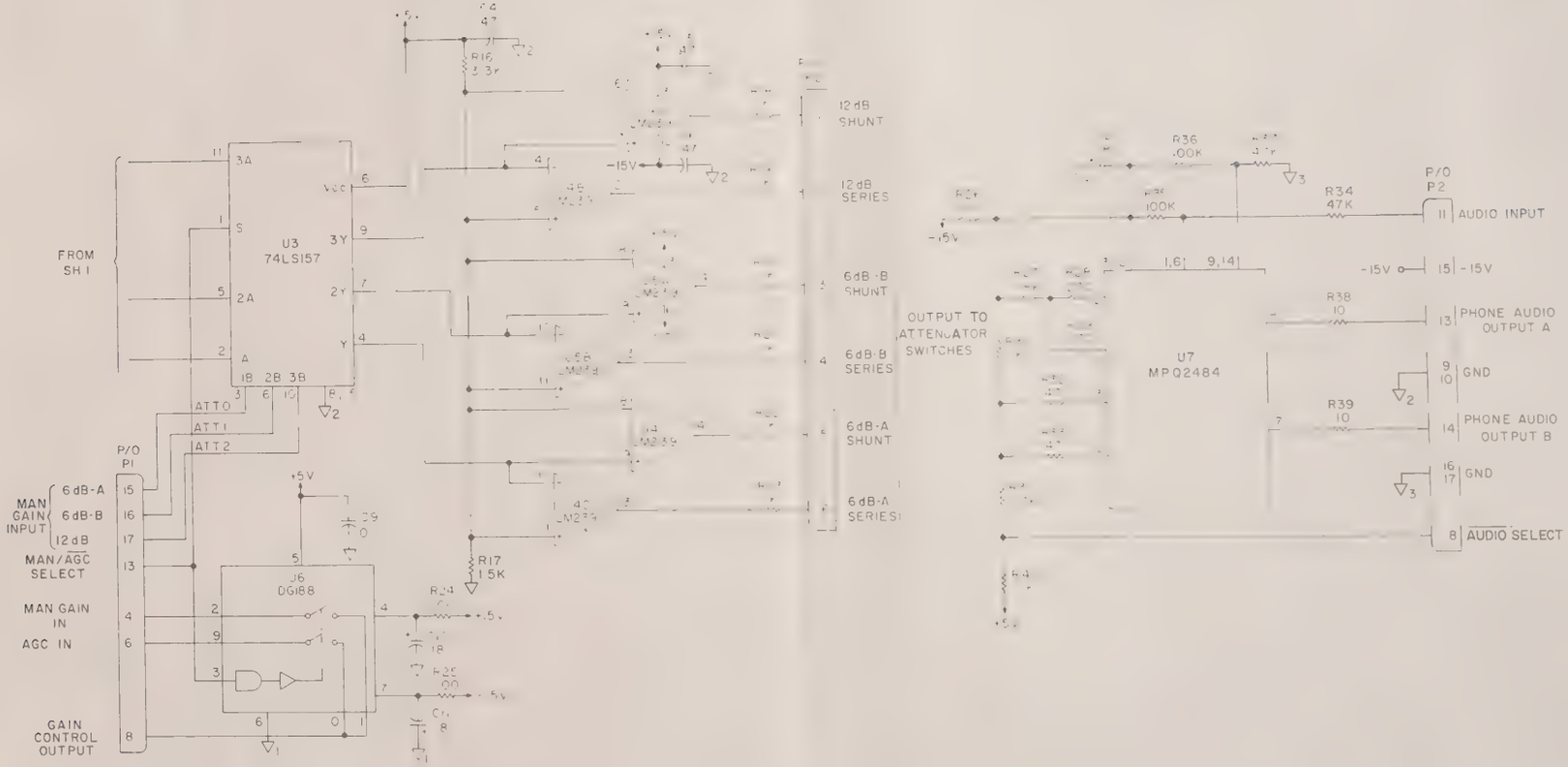


Figure 7-18. Type 796066 Attenuator Control (A3A1A5), Schematic Diagram (Sheet 2 of 2)

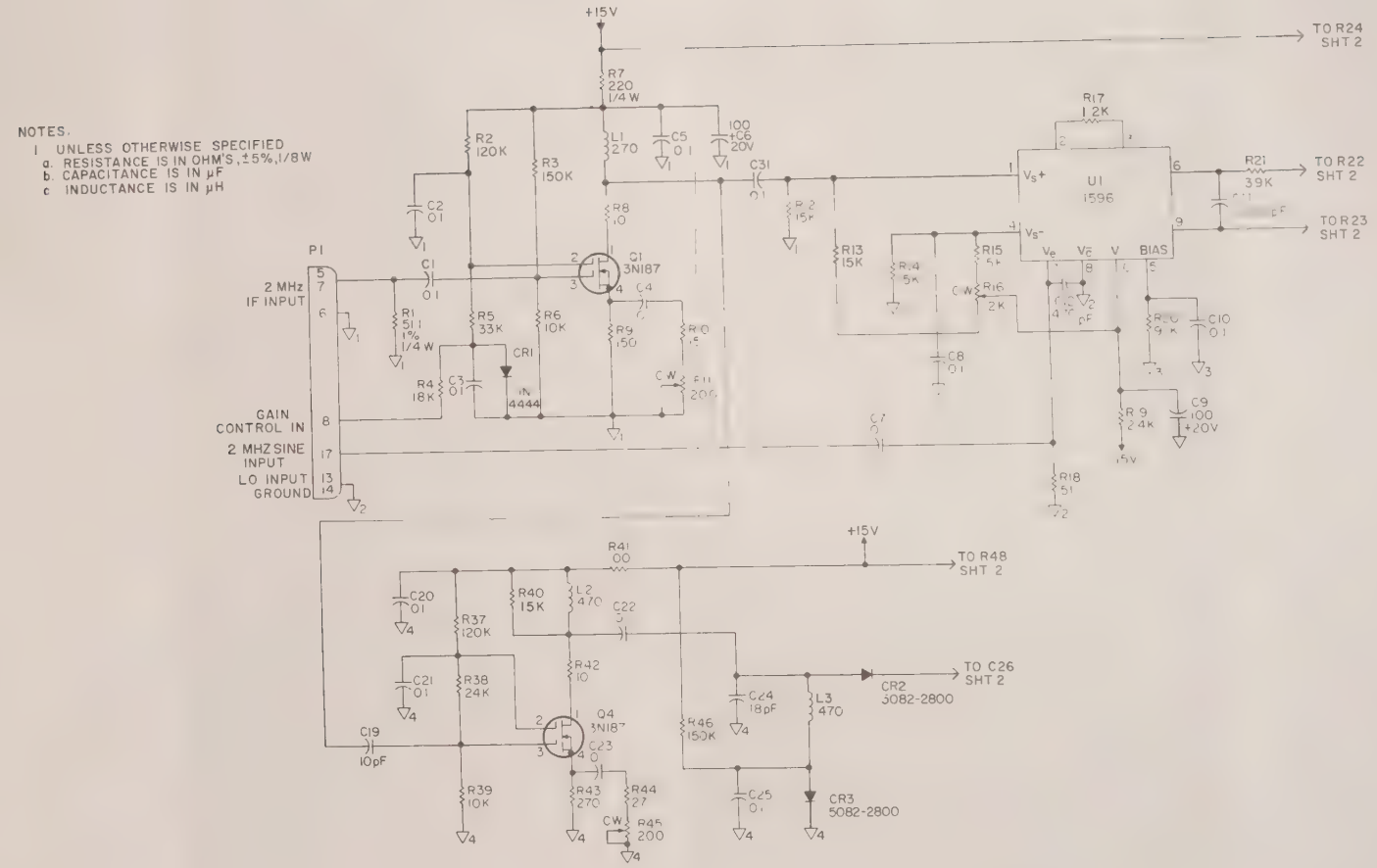


Figure 7-19. Type 796069 IF Demodulator (A3A1A6), Schematic Diagram (Sheet 1 of 2)

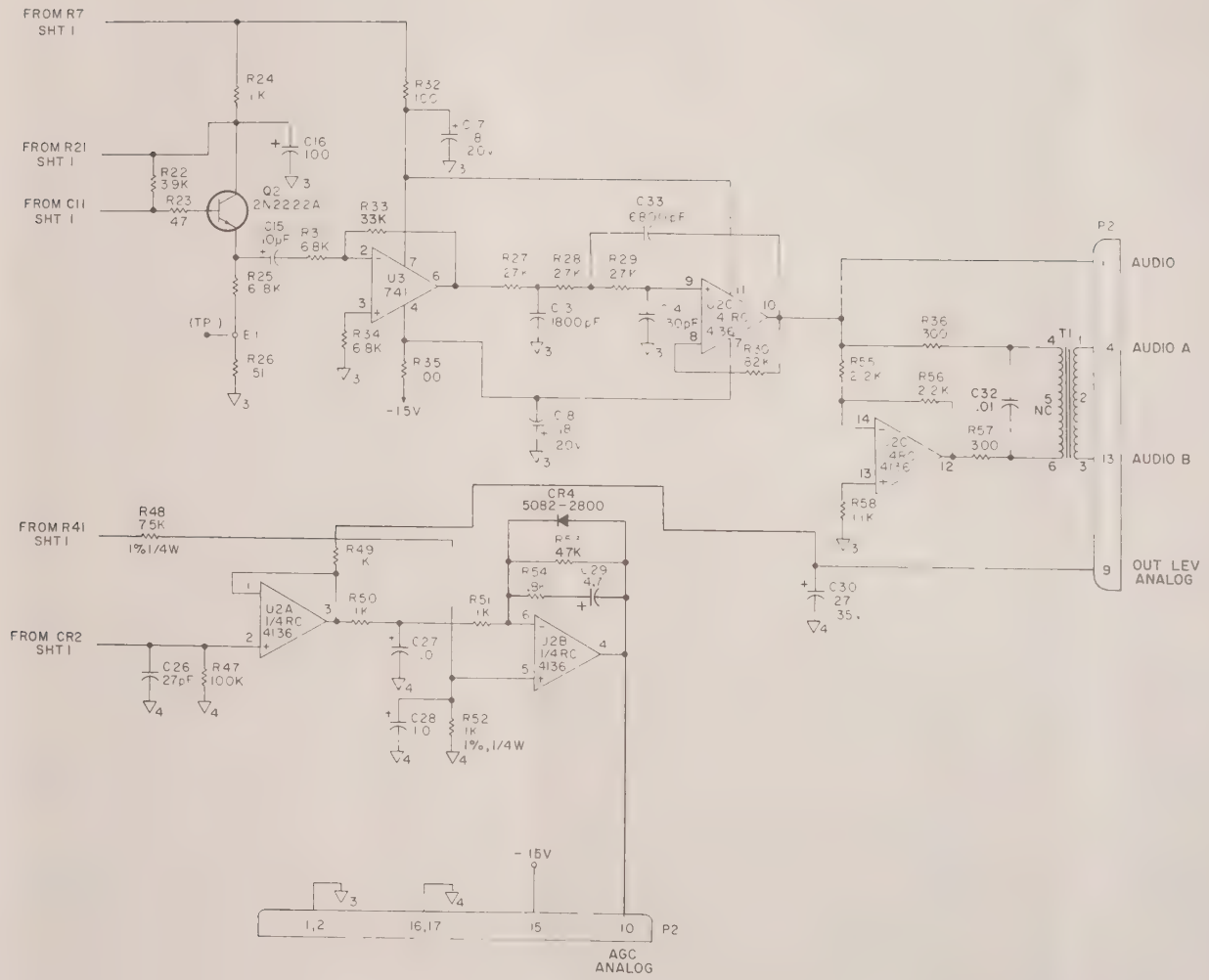
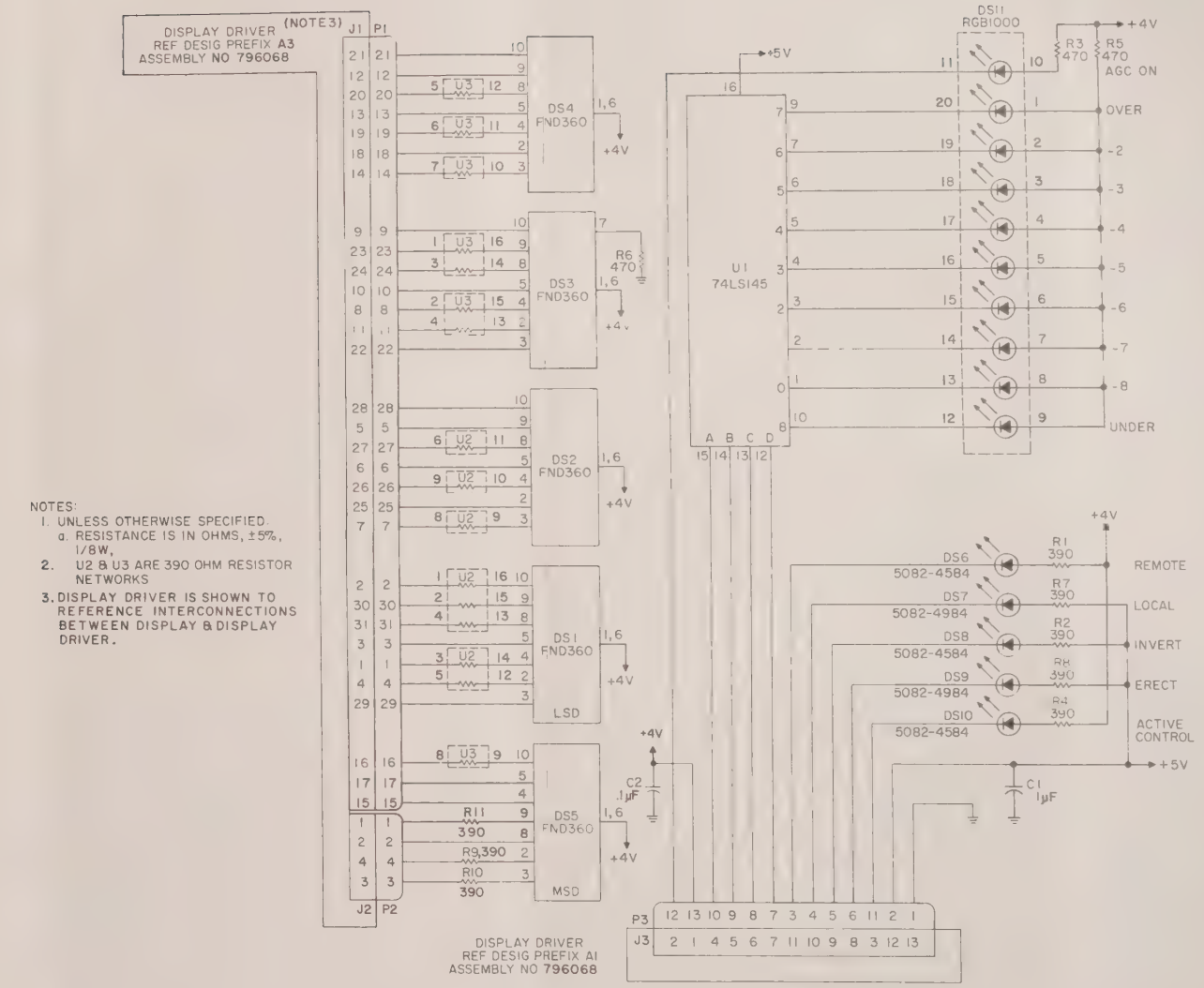
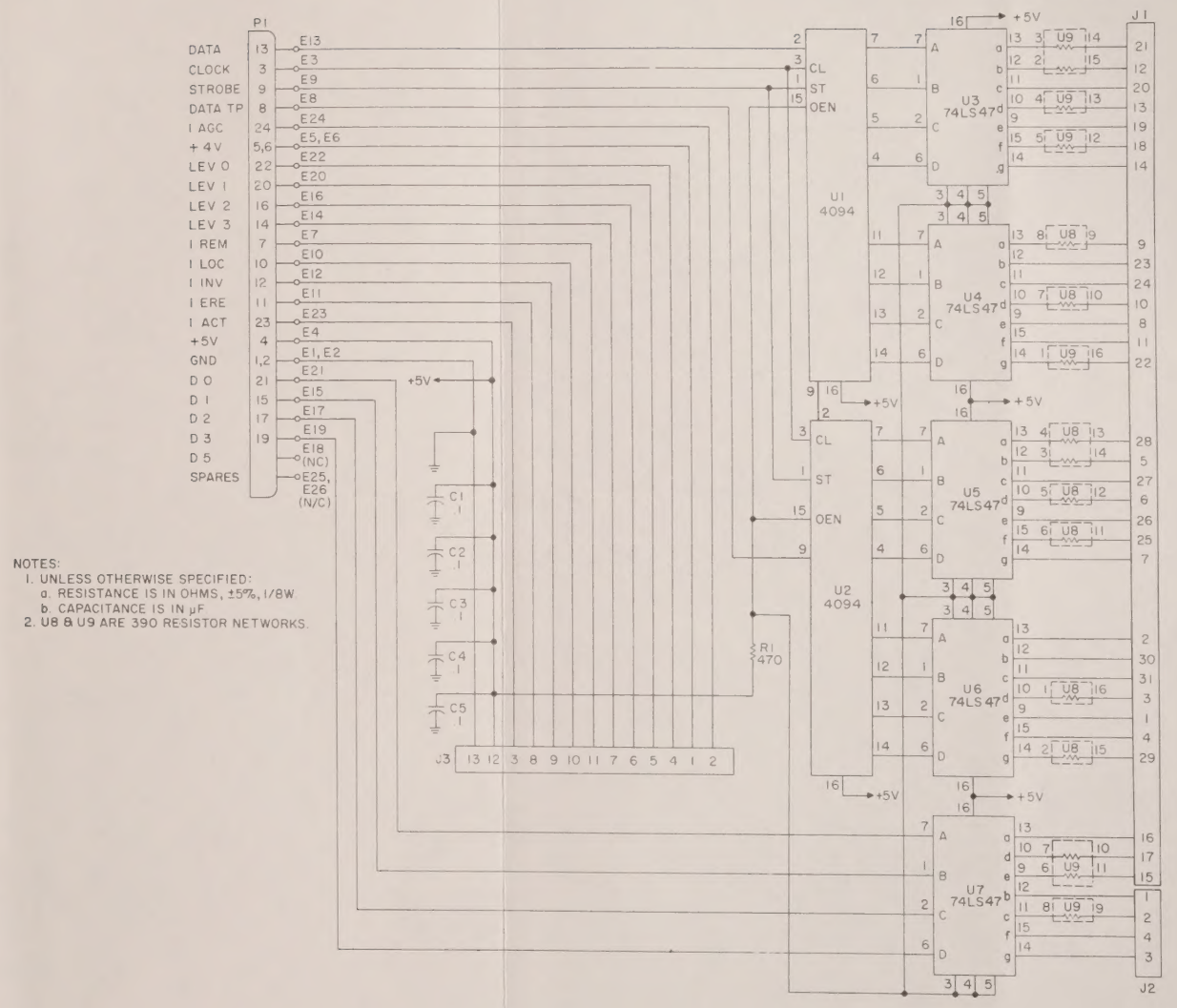


Figure 7-19. Type 796069 IF Demodulator (A3A1A6), Schematic Diagram (Sheet 2 of 2)



NOTES:
1. UNLESS OTHERWISE SPECIFIED.
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W,
2. U2 & U3 ARE 390 OHM RESISTOR NETWORKS
3. DISPLAY DRIVER IS SHOWN TO REFERENCE INTERCONNECTIONS BETWEEN DISPLAY & DISPLAY DRIVER.

Figure 7-20. Type 796067 Display Board (A3A2), Schematic Diagram



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b. CAPACITANCE IS IN μF.
2. U8 & U9 ARE 390 RESISTOR NETWORKS.

Figure 7-21. Type 796068 Display Driver (A3A3), Schematic Diagram

MP MASTER
MA31062